

# **Intel® Core™2 Duo Processors and Intel® Core™2 Extreme Processors for Platforms Based on Mobile Intel® 965 Express Chipset Family**

**Datasheet**

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*January 2008*



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## Revision History

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Document Number	Revision Number	Description	Date
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# 1 Introduction

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The Intel® Core™2 Duo processor on 65-nm process technology is the next generation high-performance, low-power processor based on the Intel® Core™ microarchitecture. The Intel Core 2 Duo processor supports the Mobile Intel® 965 Express Chipset and Intel® 82801HBM ICH8M Controller Hub Based Systems. This document contains electrical, mechanical and thermal specifications for the following processors:

- Intel Core 2 Duo processor - Standard Voltage
- Intel Core 2 Duo processor - Low Voltage
- Intel Core 2 Duo processor - Ultra Low Voltage
- Intel Core 2 Extreme processor

**Note:** In this document, the Intel Core 2 Duo and Intel Core 2 Extreme processors are referred to as the processor and Mobile Intel® 965 Express Chipset family is referred to as the (G)MCH.

The following list provides some of the key features on this processor:

- Dual core processor for mobile with enhanced performance
- Intel architecture with Intel® Wide Dynamic Execution
- L1 Cache to Cache (C2C) transfer
- On-die, primary 32-KB instruction cache and 32-KB write-back data cache in each core
- On-die, up to 4-MB second level shared cache with advanced transfer cache architecture
- Streaming SIMD Extensions 2 (SSE2), Streaming SIMD Extensions 3 (SSE3) and Supplemental Streaming SIMD Extensions 3 (SSSE3)
- 800-MHz Source-Synchronous Front Side Bus (FSB) for Intel Core 2 Extreme processors, Intel Core 2 Duo standard and low voltage processors. 533-MHz FSB for Intel Core 2 Duo ultra low voltage processors
- Advanced power management features including Enhanced Intel SpeedStep® Technology and Dynamic FSB frequency switching.
- Intel Enhanced Deeper Sleep state with P\_LVL5 I/O support
- Digital Thermal Sensor (DTS)
- Intel® 64 Technology
- Enhanced Intel® Virtualization Technology
- Intel® Dynamic Acceleration Technology
- Enhanced Multi Threaded Thermal Management (EMTTM)
- PSI2 functionality
- Standard voltage processors are offered in Micro-FCPGA and Micro-FCBGA packaging. Low voltage and Ultra low voltage processors are offered in Micro-FCBGA packaging only. Intel Core 2 Extreme processors are offered in Micro-FCPGA packaging only.
- Execute Disable Bit support for enhanced security

## 1.1 Terminology

Term	Definition
#	A “#” symbol after a signal name refers to an active low signal, indicating a signal is in the active state when driven to a low level. For example, when RESET# is low, a reset has been requested. Conversely, when NMI is high, a nonmaskable interrupt has occurred. In the case of signals where the name does not imply an active state but describes part of a binary sequence (such as <i>address</i> or <i>data</i> ), the “#” symbol implies that the signal is inverted. For example, D[3:0] = “HLHL” refers to a hex ‘A’, and D[3:0]# = “LHLH” also refers to a hex “A” (H= High logic level, L= Low logic level). XXXX means that the specification or value is yet to be determined.
Front Side Bus (FSB)	Refers to the interface between the processor and system core logic (also known as the chipset components).
AGTL+	Advanced Gunning Transceiver Logic. Used to refer to Assisted GTL+ signaling technology on some Intel processors.
Storage Conditions	Refers to a non-operational state. The processor may be installed in a platform, in a tray, or loose. Processors may be sealed in packaging or exposed to free air. Under these conditions, processor landings should not be connected to any supply voltages, have any I/Os biased or receive any clocks. Upon exposure to “free air” (i.e., unsealed packaging or a device removed from packaging material) the processor must be handled in accordance with moisture sensitivity labeling (MSL) as indicated on the packaging material.
Enhanced Intel SpeedStep® Technology	Technology that provides power management capabilities to laptops.
Processor Core	Processor core die with integrated L1 and L2 cache. All AC timing and signal integrity specifications are at the pads of the processor core.
Intel® 64 Technology	64-bit memory extensions to the IA-32 architecture.
Intel® Virtualization Technology	Processor virtualization which when used in conjunction with Virtual Machine Monitor software enables multiple, robust independent software environments inside a single platform.
TDP	Thermal Design Power
V <sub>CC</sub>	The processor core power supply
V <sub>SS</sub>	The processor ground





## 1.2 References

Material and concepts available in the following documents may be beneficial when reading this document.

Document	Document Number <sup>1,2</sup>
<i>Intel® Core™ 2 Duo Processors For Intel® Centrino® Duo Processor Technology Specification Update</i>	314079
<i>Mobile Intel® 965 Express Chipset Family Datasheet</i>	316273
<i>Mobile Intel® 965 Express Chipset Family Specification Update</i>	316274
<i>Intel® I/O Controller Hub 8 (ICH8)/ I/O Controller Hub 8M (ICH8M) Datasheet</i>	See <a href="http://www.intel.com/design/chipsets/datashts/313056.htm">http://www.intel.com/design/chipsets/datashts/313056.htm</a>
<i>Intel® I/O Controller Hub 8 (ICH8)/ I/O Controller Hub 8M (ICH8M) Specification Update</i>	See <a href="http://www.intel.com/design/chipsets/specupdt/313057.htm">http://www.intel.com/design/chipsets/specupdt/313057.htm</a>
<i>Intel® 64 and IA-32 Architectures Software Developer's Manual</i>	See <a href="http://www.intel.com/design/pentium4/manuals/index_new.htm">http://www.intel.com/design/pentium4/manuals/index_new.htm</a>
<i>Intel® 64 and IA-32 Architectures Software Developer's Manuals Documentation Change</i>	See <a href="http://developer.intel.com/design/processor/specupdt/252046.htm">http://developer.intel.com/design/processor/specupdt/252046.htm</a>
<i>Volume 1: Basic Architecture</i>	253665
<i>Volume 2A: Instruction Set Reference, A-M</i>	253666
<i>Volume 2B: Instruction Set Reference, N-Z</i>	253667
<i>Volume 3A: System Programming Guide</i>	253668
<i>Volume 3B: System Programming Guide</i>	253669

### NOTES:

1. Contact your local Intel representative for the latest revision of this document.





## 2 Low Power Features

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### 2.1 Clock Control and Low Power States

The processor supports low power states both at the individual core level and the package level for optimal power management.

A core may independently enter the C1/AutoHALT, C1/MWAIT, C2, C3, and C4 low power states. When both cores coincide in a common core low power state, the central power management logic ensures that the entire processor enters the respective package low power state by initiating a P\_LVLx (P\_LVL2, P\_LVL3, P\_LVL4, or P\_LVL5) I/O read to the chipset.

The processor implements two software interfaces for requesting low power states: MWAIT instruction extensions with sub-state hints or P\_LVLx reads to the ACPI P\_BLK register block mapped in the processor's I/O address space. The P\_LVLx I/O reads are converted to equivalent MWAIT C-state requests inside the processor and do not directly result in I/O reads on the processor FSB. The P\_LVLx I/O monitor address does not need to be set up before using the P\_LVLx I/O read interface. The sub-state hints used for each P\_LVLx read can be configured through the Model Specific Register (MSR).

If a core encounters a chipset break event while STPCLK# is asserted, then it asserts the PBE# output signal. Assertion of PBE# when STPCLK# is asserted indicates to system logic that individual cores should return to the C0 state and the processor should return to the Normal state.

[Figure 1](#) shows the core low power states and [Figure 2](#) shows the package low power states. [Table 1](#) maps the core low power states to the package low power states.

Figure 1. Core Low Power States

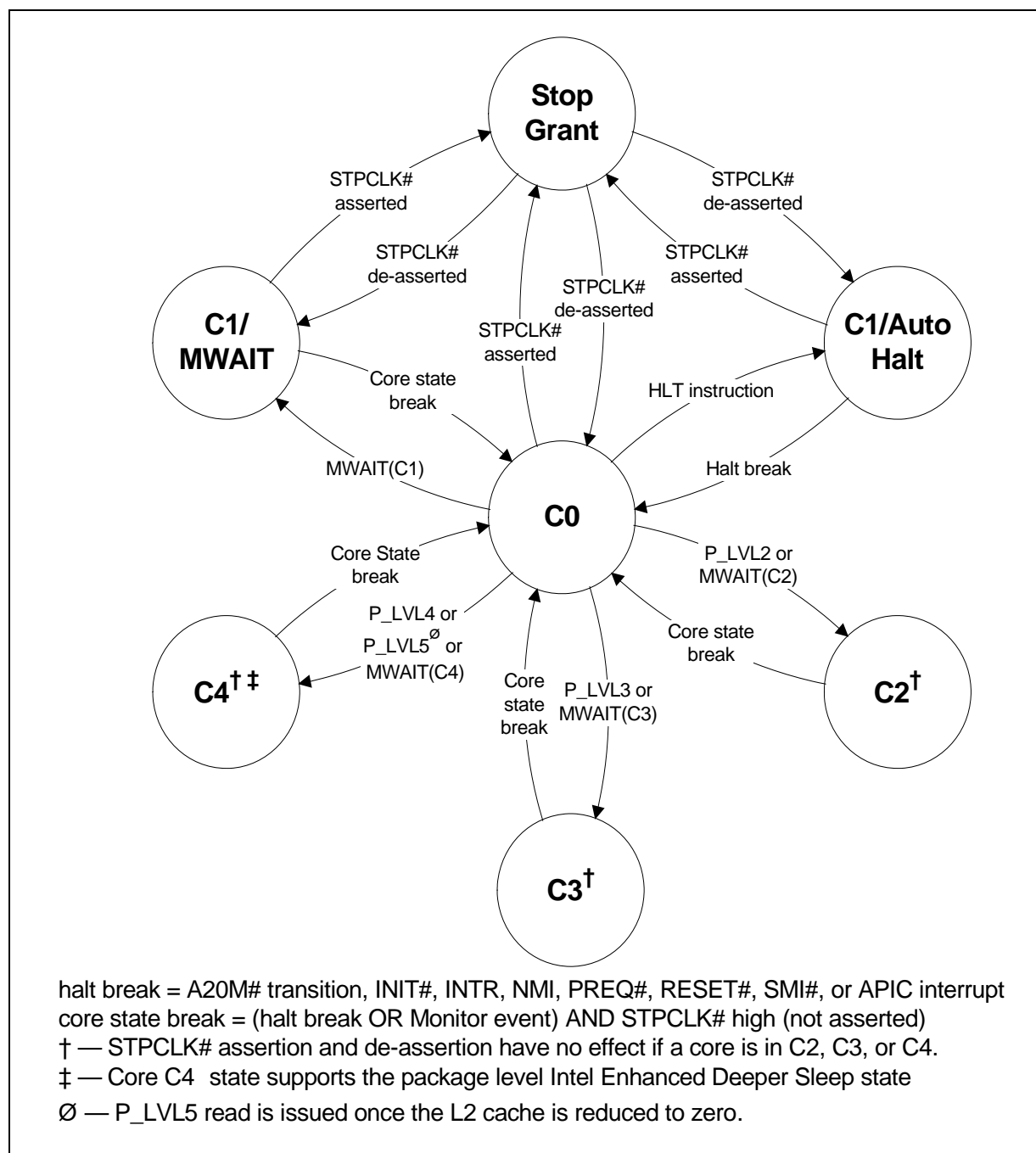




Figure 2. Package Low Power States

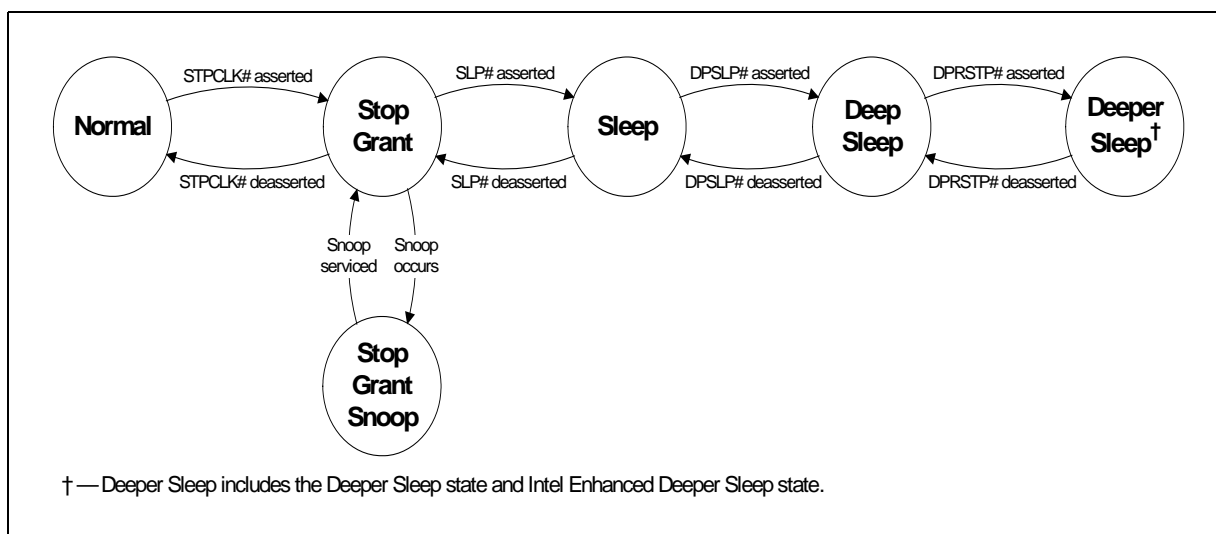


Table 1. Coordination of Core Low Power States at the Package Level

Package State	Core1 State				
Core0 State	C0	C1 <sup>1</sup>	C2	C3	C4
C0	Normal	Normal	Normal	Normal	Normal
C1 <sup>1</sup>	Normal	Normal	Normal	Normal	Normal
C2	Normal	Normal	Stop-Grant	Stop Grant	Stop Grant
C3	Normal	Normal	Stop-Grant	Deep Sleep	Deep Sleep
C4	Normal	Normal	Stop-Grant	Deep Sleep	Deeper Sleep / Intel® Enhanced Deeper Sleep

**NOTES:**

1. AutoHALT or MWAIT/C1.

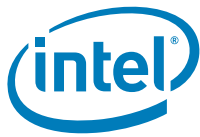
## 2.1.1 Core Low Power State Descriptions

### 2.1.1.1 Core C0 State

This is the normal operating state for cores in the processor.

### 2.1.1.2 Core C1/AutoHALT Powerdown State

C1/AutoHALT is a low power state entered when a core executes the HALT instruction. The processor transitions to the C0 state upon occurrence of SMI#, INIT#, LINT[1:0] (NMI, INTR), or FSB interrupt messages. RESET# causes the processor to immediately initialize itself.



A System Management Interrupt (SMI) handler returns execution to either Normal state or the AutoHALT Powerdown state. See the *Intel® 64 and IA-32 Architectures Software Developer's Manual, Volume 3A/3B: System Programmer's Guide* for more information.

The system can generate a STPCLK# while the processor is in the AutoHALT Powerdown state. When the system deasserts the STPCLK# interrupt, the processor returns execution to the HALT state.

While in AutoHALT Powerdown state, the dual core processor processes bus snoops and snoops from the other core. The processor enters a snoopable sub-state (not shown in [Figure 1](#)) to process the snoop and then return to the AutoHALT Powerdown state.

### 2.1.1.3 Core C1/MWAIT Powerdown State

C1/MWAIT is a low power state entered when the processor core executes the MWAIT(C1) instruction. Processor behavior in the MWAIT state is identical to the AutoHALT state except that Monitor events can cause the processor core to return to the C0 state. See the *Intel® 64 and IA-32 Architectures Software Developer's Manual, Volume 2A: Instruction Set Reference, A-M* and *Volume 2B: Instruction Set Reference, N-Z*, for more information.

### 2.1.1.4 Core C2 State

Individual cores of the dual core processor can enter the C2 state by initiating a P\_LVL2 I/O read to the P\_BLK or an MWAIT(C2) instruction, but the processor does not issue a Stop-Grant Acknowledge special bus cycle unless the STPCLK# pin is also asserted.

While in the C2 state, the dual core processor processes bus snoops and snoops from the other core. The processor enters a snoopable sub-state (not shown in [Figure 1](#)) to process the snoop and then return to the C2 state.

### 2.1.1.5 Core C3 State

Individual cores of the dual core processor can enter the C3 state by initiating a P\_LVL3 I/O read to the P\_BLK or an MWAIT(C3) instruction. Before entering C3, the processor core flushes the contents of its L1 caches into the processor's L2 cache. Except for the caches, the processor core maintains all its architectural state in the C3 state. The monitor remains armed if it is configured. All of the clocks in the processor core are stopped in the C3 state.

Because the core's caches are flushed the processor keeps the core in the C3 state when the processor detects a snoop on the FSB or when the other core of the dual core processor accesses cacheable memory. The processor core transitions to the C0 state upon occurrence of a Monitor event, SMI#, INIT#, LINT[1:0] (NMI, INTR), or FSB interrupt message. RESET# causes the processor to immediately initialize itself.

### 2.1.1.6 Core C4 State

Individual cores of the dual core processor can enter the C4 state by initiating a P\_LVL4 I/O read to the P\_BLK or an MWAIT(C4) instruction. The processor core behavior in the C4 state is nearly identical to the behavior in the C3 state. The only difference is that if both processor cores are in C4, then the central power management logic requests that the entire processor enter the Deeper Sleep package low power state (see [Section 2.1.2.6](#)).

To enable the package level Intel Enhanced Deeper Sleep state, Dynamic Cache Sizing and Intel Enhanced Deeper Sleep state fields must be configured in the software programmable MSR. Refer to [Section 2.1.2.6](#) for further details on Intel Enhanced Deeper Sleep state.



## 2.1.2 Package Low Power State Descriptions

### 2.1.2.1 Normal State

This is the normal operating state for the processor. The processor remains in the Normal state when at least one of its cores is in the C0, C1/AutoHALT, or C1/MWAIT state.

### 2.1.2.2 Stop-Grant State

When the STPCLK# pin is asserted by the chipset, each core of the dual core processor enters the Stop-Grant state within 20-bus clocks after the response phase of the processor-issued Stop-Grant Acknowledge special bus cycle. Processor cores that are already in the C2, C3, or C4 state remain in their current low power state. When the STPCLK# pin is deasserted, each core returns to its previous core low power state.

Since the AGTL+ signal pins receive power from the FSB, these pins should not be driven (allowing the level to return to  $V_{CCP}$ ) for minimum power drawn by the termination resistors in this state. In addition, all other input pins on the FSB should be driven to the inactive state.

RESET# causes the processor to immediately initialize itself, but the processor stays in Stop-Grant state. When RESET# is asserted by the system, the STPCLK#, SLP#, DPSTP#, and DPRSTP# pins must be deasserted prior to RESET# deassertion. When re-entering the Stop-Grant state from the Sleep state, STPCLK# should be deasserted after the deassertion of SLP#.

While in Stop-Grant state, the processor services snoops and latch interrupts delivered on the FSB. The processor latches SMI#, INIT# and LINT[1:0] interrupts and services only one of each upon return to the Normal state.

The PBE# signal may be driven when the processor is in Stop-Grant state. PBE# asserts if there is any pending interrupt or Monitor event latched within the processor. Pending interrupts that are blocked by the EFLAGS.IF bit being clear causes assertion of PBE#. Assertion of PBE# indicates to system logic that the entire processor should return to the Normal state.

A transition to the Stop-Grant Snooze state occurs when the processor detects a snoop on the FSB (see [Section 2.1.2.3](#)). A transition to the Sleep state (see [Section 2.1.2.4](#)) occurs with the assertion of the SLP# signal.

### 2.1.2.3 Stop-Grant Snooze State

The processor responds to snoop or interrupt transactions on the FSB while in Stop-Grant state by entering the Stop-Grant Snooze state. The processor stays in this state until the snoop on the FSB has been serviced (whether by the processor or another agent on the FSB) or the interrupt has been latched. The processor returns to the Stop-Grant state once the snoop has been serviced or the interrupt has been latched.

### 2.1.2.4 Sleep State

The Sleep state is a low power state in which the processor maintains its context, maintains the phase-locked loop (PLL), and stops all internal clocks. The Sleep state is entered through assertion of the SLP# signal while in the Stop-Grant state. The SLP# pin should only be asserted when the processor is in the Stop-Grant state. SLP# assertions while the processor is not in the Stop-Grant state is out of specification and may result in unapproved operation.

In the Sleep state, the processor is incapable of responding to snoop transactions or latching interrupt signals. No transitions or assertions of signals (with the exception of SLP#, DPSLP# or RESET#) are allowed on the FSB while the processor is in Sleep state. Snoop events that occur while in Sleep state or during a transition into or out of Sleep state causes unpredictable behavior. Any transition on an input signal before the processor has returned to the Stop-Grant state results in unpredictable behavior.

If RESET# is driven active while the processor is in the Sleep state, and held active, then the processor resets itself, ignoring the transition through Stop-Grant state. If RESET# is driven active while the processor is in the Sleep state, the SLP# and STPCLK# signals should be deasserted immediately after RESET# is asserted to ensure the processor correctly executes the Reset sequence.

While in the Sleep state, the processor is capable of entering an even lower power state, the Deep Sleep state, by asserting the DPSLP# pin (See [Section 2.1.2.5](#)). While the processor is in the Sleep state, the SLP# pin must be deasserted if another asynchronous FSB event needs to occur.

#### 2.1.2.5 Deep Sleep State

The Deep Sleep state is entered through assertion of the DPSLP# pin while in the Sleep state. BCLK may be stopped during the Deep Sleep state for additional platform-level power savings. BCLK stop/restart timings on appropriate chipset based platforms with the CK505 clock chip are as follows:

- Deep Sleep entry: the system clock chip may stop/tristate BCLK within 2 BCLKs of DPSLP# assertion. It is permissible to leave BCLK running during Deep Sleep.
- Deep Sleep exit: the system clock chip must drive BCLK to differential DC levels within 2-3 ns of DPSLP# deassertion and start toggling BCLK within 10 BCLK periods.

To re-enter the Sleep state, the DPSLP# pin must be deasserted. BCLK can be re-started after DPSLP# deassertion as described above. A period of 15 microseconds (to allow for PLL stabilization) must occur before the processor can be considered to be in the Sleep state. Once in the Sleep state, the SLP# pin must be deasserted to re-enter the Stop-Grant state.

While in Deep Sleep state, the processor is incapable of responding to snoop transactions or latching interrupt signals. No transitions of signals are allowed on the FSB while the processor is in Deep Sleep state. When the processor is in Deep Sleep state, it does not respond to interrupts or snoop transactions. Any transition on an input signal before the processor has returned to Stop-Grant state results in unpredictable behavior.

#### 2.1.2.6 Deeper Sleep State

The Deeper Sleep state is similar to the Deep Sleep state but further reduces core voltage levels. One of the potential lower core voltage levels is achieved by entering the base Deeper Sleep state. The Deeper Sleep state is entered through assertion of the DPRSTP# pin while in the Deep Sleep state. The other lower core voltage level, the lowest possible in the processor, is achieved by entering the Intel Enhanced Deeper Sleep state which is a sub-state of Deeper Sleep state. Intel Enhanced Deeper Sleep state is entered through assertion of the DPRSTP# pin while in the Deep Sleep only when the L2 cache has been completely shut down. Refer to [Section 2.1.2.6.1](#) and [Section 2.1.2.6.2](#) for further details on reducing the L2 cache and entering Intel Enhanced Deeper Sleep state.

In response to entering Deeper Sleep, the processor drives the VID code corresponding to the Deeper Sleep core voltage on the VID[6:0] pins.





Exit from Deeper Sleep or Intel Enhanced Deeper Sleep state is initiated by DPRSTP# deassertion when either core requests a core state other than C4 or either core requests a processor performance state other than the lowest operating point.

#### 2.1.2.6.1 Intel Enhanced Deeper Sleep State

Intel Enhanced Deeper Sleep state is a sub-state of Deeper Sleep that extends power-saving capabilities by allowing the processor to further reduce core voltage once the L2 cache has been reduced to zero ways and completely shut down. The following events occur when the processor enters Intel Enhanced Deeper Sleep state:

- The last core entering C4 causes the package to issue a P\_LVL4 IO Read.
- Every concurrent package C4 entry reduces the L2 Cache a certain number of cache ways, after which another P\_LVL4 IO Read is issued to the chipset. By default, half the cache is flushed per concurrent C4 entry.
- Once the cache is flushed, P\_LVL4 IO Reads continue to be issued.
- The processor drives the VID code corresponding to the Intel Enhanced Deeper Sleep state core voltage on the VID[6:0] pins.

At this point, snoops to the L2 are still serviced, which reduces the amount of time the processor can reside at the Intel Enhanced Deeper Sleep state core voltage.

To improve the Intel Enhanced Deeper Sleep state residency, the (G)MCH features P\_LVL5 IO Read support. When enabled, the CPU issues a P\_LVL5 IO read, once the L2 cache is flushed. The P\_LVL5 IO read triggers a special chipset sequence to notify the chipset to redirect all FSB traffic, except APIC messages, to memory instead of L2 cache. Therefore, the processor remains at the Intel Enhanced Deeper Sleep state core voltage for a longer period of time.

#### 2.1.2.6.2 Dynamic Cache Sizing

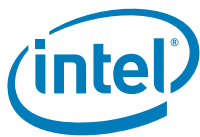
Dynamic Cache Sizing allows the processor to flush and disable a programmable number of L2 cache ways upon each Deeper Sleep entry under the following conditions:

- The second core is already in C4 and the Intel Enhanced Deeper Sleep state is enabled (as specified in [Section 2.1.1.6](#)).
- The C0 timer, which tracks continuous residency in the Normal package state, has not expired. This timer is cleared during the first entry into Deeper Sleep to allow consecutive Deeper Sleep entries to shrink the L2 cache as needed.
- The FSB speed to processor core speed ratio is below the predefined L2 shrink threshold.

If the FSB speed to processor core speed ratio is above the predefined L2 shrink threshold, then L2 cache expansion is requested. If the ratio is zero, then the ratio is not taken into account for Dynamic Cache Sizing decisions.

Upon STPCLK# deassertion, the first core exiting Intel Enhanced Deeper Sleep state expands the L2 cache to two ways and invalidate previously disabled cache ways. If the L2 cache reduction conditions stated above still exist when the last core returns to C4 and the package enters Intel Enhanced Deeper Sleep state, then the L2 is shrunk to zero again. If a core requests a processor performance state resulting in a higher ratio than the predefined L2 shrink threshold, the C0 timer expires, or the second core (not the one currently entering the interrupt routine) requests the C1, C2, or C3 states, then all of L2 expands upon the next interrupt event.

L2 cache shrink prevention may be enabled as needed on occasion through an MWAIT(C4) sub-state field. If shrink prevention is enabled the processor does not enter Intel Enhanced Deeper Sleep state because the L2 cache remains valid and in full size.



## 2.2 Enhanced Intel SpeedStep® Technology

The processor features Enhanced Intel SpeedStep Technology. Following are the key features of Enhanced Intel SpeedStep Technology:

- Multiple voltage and frequency operating points provide optimal performance at the lowest power.
- Voltage and frequency selection is software-controlled by writing to processor MSRs:
  - If the target frequency is higher than the current frequency, V<sub>CC</sub> is ramped up in steps by placing new values on the VID pins, and the PLL then locks to the new frequency.
  - If the target frequency is lower than the current frequency, the PLL locks to the new frequency, and the V<sub>CC</sub> is changed through the VID pin mechanism.
  - Software transitions are accepted at any time. If a previous transition is in progress the new transition is deferred until the previous transition completes.
- The processor controls voltage ramp rates internally to ensure glitch-free transitions.
- Low transition latency and large number of transitions possible per second:
  - Processor core (including L2 cache) is unavailable for up to 10 ms during the frequency transition.
  - The bus protocol (BNR# mechanism) is used to block snooping.
- Improved Intel® Thermal Monitor mode:
  - When the on-die thermal sensor indicates that the die temperature is too high, the processor can automatically perform a transition to a lower frequency and voltage specified in a software-programmable MSR.
  - The processor waits for a fixed time period. If the die temperature is down to acceptable levels, an up-transition to the previous frequency and voltage point occurs.
  - An interrupt is generated for the up and down Intel Thermal Monitor transitions enabling better system-level thermal management.
- Enhanced thermal management features:
  - Digital Thermal Sensor and Out of Specification detection
  - Intel Thermal Monitor 1 in addition to Intel Thermal Monitor 2 in case of unsuccessful Intel Thermal Monitor 2 transition.
  - Dual core thermal management synchronization.

Each core in the dual processor implements an independent MSR for controlling Enhanced Intel SpeedStep Technology, but both cores must operate at the same frequency and voltage. The processor has performance state coordination logic to resolve frequency and voltage requests from the two cores into a single frequency and voltage request for the package as a whole. If both cores request the same frequency and voltage, then the processor transitions to the requested common frequency and voltage. If the two cores have different frequency and voltage requests, then the processor takes the highest of the two frequencies and voltages as the resolved request, and transition to that frequency and voltage.

The processor also supports Dynamic FSB Frequency Switching and Intel® Dynamic Acceleration Technology mode on select SKUs. The operating system can take advantage of these features and request a lower operating point called SuperLFM (due to Dynamic FSB Frequency Switching) and a higher operating point Intel Dynamic Acceleration Technology mode.



### 2.2.1 Dynamic FSB Frequency Switching

Dynamic FSB frequency switching effectively reduces the internal bus clock frequency in half to further decrease the minimum processor operating frequency from the Enhanced Intel SpeedStep Technology performance states and achieve the Super Low Frequency Mode (SuperLFM). This feature is supported at FSB frequencies of 800-MHz and does not entail a change in the external bus signal (BCLK) frequency. Instead, both the processor and (G)MCH internally lower their BCLK reference frequency to 50% of the externally visible frequency. Both the processor and (G)MCH maintain a virtual BCLK signal ("VBCLK") that is aligned to the external BCLK but at half the frequency. After a downward shift, it would appear externally as if the bus is running with a 100-MHz base clock in all aspects, except that the actual external BCLK remains at 200 MHz. The transition into SuperLFM, a "down-shift", is done following a handshake between the processor and (G)MCH. A similar handshake is used to indicate an "up-shift", a change back to normal operating mode.

### 2.2.2 Intel® Dynamic Acceleration Technology

The processor supports Intel Dynamic Acceleration Technology mode on select platforms. The Intel Dynamic Acceleration Technology mode feature allows one core of the processor to temporarily operate at a higher frequency point when the other core is inactive and the operating system requests increased performance. This higher frequency is called the opportunistic frequency and the maximum rated operating frequency is the guaranteed frequency.

**Note:** Intel Core 2 Extreme processors do not support Intel Dynamic Acceleration mode.

Intel Dynamic Acceleration Technology mode enabling requires:

- Exposure, via BIOS, of the opportunistic frequency as the highest ACPI P state.
- Enhanced Multi-Threaded Thermal Management (EMTTM).
- Intel Dynamic Acceleration Technology mode and EMTTM MSR configuration via BIOS.

When in Intel Dynamic Acceleration Technology mode, it is possible for both cores to be active under certain internal conditions. In such a scenario the processor may draw a Instantaneous current ( $I_{CC\_CORE\_INST}$ ) for a short duration of  $t_{INST}$ ; however, the average  $I_{CC}$  current is lesser than or equal to  $I_{CCDES}$  current specification. Please refer to the Processor DC Specifications section for more details.

## 2.3 Extended Low Power States

Extended low power states (CxE) optimize for power by forcibly reducing the performance state of the processor when it enters a package low power state. Instead of directly transitioning into the package low power state, the extended package low power state first reduces the performance state of the processor by performing an Enhanced Intel SpeedStep Technology transition down to the lowest operating point. Upon receiving a break event from the package low power state, control returns to the software while an Enhanced Intel SpeedStep Technology transition up to the initial operating point occurs. The advantage of this feature is that it significantly reduces leakage while in low power states.

**Note:** Long-term reliability cannot be assured unless all the Extended Low Power states are enabled.



The processor implements two software interfaces for requesting extended package low power states: MWAIT instruction extensions with sub-state hints and via BIOS by configuring MSR bits to automatically promote package low power states to extended package low power states.

**Extended Stop-Grant and Extended Deeper Sleep must be enabled via the BIOS for the processor to remain within specification.** Any attempt to operate the processor outside these operating limits may result in permanent damage to the processor. As processor technology changes, enabling the extended low power states becomes increasingly crucial when building computer systems. Maintaining the proper BIOS configuration is key to reliable, long-term system operation. Not complying with this guideline may affect the long-term reliability of the processor.

Enhanced Intel SpeedStep Technology transitions are multistep processes that require clocked control. These transitions cannot occur when the processor is in the Sleep or Deep Sleep package low power states since processor clocks are not active in these states. Extended Deeper Sleep state configuration lowers core voltage to the Deeper Sleep level while in Deeper Sleep and, upon exit, automatically transitions to the lowest operating voltage and frequency to reduce snoop service latency. The transition to the lowest operating point or back to the original software requested point may not be instantaneous. Furthermore, upon very frequent transitions between active and idle states, the transitions may lag behind the idle state entry resulting in the processor either executing for a longer time at the lowest operating point or running idle at a high operating point. Observations and analyses show this behavior should not significantly impact total power savings or performance score while providing power benefits in most other cases.

## 2.4 FSB Low Power Enhancements

The processor incorporates FSB low power enhancements:

- Dynamic FSB Power Down
- BPRI# control for address and control input buffers
- Dynamic Bus Parking
- Dynamic On Die Termination disabling
- Low  $V_{CCP}$  (I/O termination voltage)

The processor incorporates the DPWR# signal that controls the data bus input buffers on the processor. The DPWR# signal disables the buffers when not used and activates them only when data bus activity occurs, resulting in significant power savings with no performance impact. BPRI# control also allows the processor address and control input buffers to be turned off when the BPRI# signal is inactive. Dynamic Bus Parking allows a reciprocal power reduction in chipset address and control input buffers when the processor deasserts its BRO# pin. The On Die Termination on the processor FSB buffers is disabled when the signals are driven low, resulting in additional power savings. The low I/O termination voltage is on a dedicated voltage plane, independent of the core voltage, enabling low I/O switching power at all times.

## 2.5 VID-x

**The processor implements the VID-x feature when in Intel Dynamic Acceleration Technology mode.** VID-x provides the ability for the processor to request core voltage level reductions greater than one VID tick. The quantity of VID ticks to be reduced depends on the specific performance state in which the processor is running. This improved voltage regulator efficiency during periods of reduced power



consumption allows for leakage current reduction, which results in platform power savings and extended battery life. There is no platform-level change required to support this feature as long as the VR vendor supports the VID-x feature.

## 2.6 Processor Power Status Indicator (PSI-2) Signal

The processor incorporates the PSI# signal that is asserted when the processor is in a reduced power consumption state. PSI# can be used to improve intermediate and light load efficiency of the voltage regulator, resulting in platform power savings and extended battery life. The algorithm that the processor uses for determining when to assert PSI# is different from the algorithm used in previous mobile processors. PSI-2 functionality improves overall voltage regulator efficiency over a wide power range based on the C-state and P-state of the two cores. The combined C-state and P-state of both cores are used to dynamically predict processor power. PSI-2 functionality is expanded further to support three processor states:

- Both cores are in idle state
- Only one core is in active state
- Both cores are in active state

§





## 3 Electrical Specifications

### 3.1 Power and Ground Pins

For clean, on-chip power distribution, the processor has a large number of  $V_{CC}$  (power) and  $V_{SS}$  (ground) inputs. All power pins must be connected to  $V_{CC}$  power planes while all  $V_{SS}$  pins must be connected to system ground planes. Use of multiple power and ground planes is recommended to reduce  $I \cdot R$  drop. The processor  $V_{CC}$  pins must be supplied the voltage determined by the VID (Voltage ID) pins.

### 3.2 FSB Clock (BCLK[1:0]) and Processor Clocking

BCLK[1:0] directly controls the FSB interface speed as well as the core frequency of the processor. As in previous generation processors, the processor core frequency is a multiple of the BCLK[1:0] frequency. The processor uses a differential clocking implementation.

### 3.3 Voltage Identification

The processor uses seven voltage identification pins, VID[6:0], to support automatic selection of power supply voltages. The VID pins for processor are CMOS outputs driven by the processor VID circuitry. Table 2 specifies the voltage level corresponding to the state of VID[6:0]. A 1 refers to a high-voltage level and a 0 refers to low-voltage level.

Table 2. Voltage Identification Definition (Sheet 1 of 4)

VID6	VID5	VID4	VID3	VID2	VID1	VID0	$V_{CC}$ (V)
0	0	0	0	0	0	0	1.5000
0	0	0	0	0	0	1	1.4875
0	0	0	0	0	1	0	1.4750
0	0	0	0	0	1	1	1.4625
0	0	0	0	1	0	0	1.4500
0	0	0	0	1	0	1	1.4375
0	0	0	0	1	1	0	1.4250
0	0	0	0	1	1	1	1.4125
0	0	0	1	0	0	0	1.4000
0	0	0	1	0	0	1	1.3875
0	0	0	1	0	1	0	1.3750
0	0	0	1	0	1	1	1.3625
0	0	0	1	1	0	0	1.3500
0	0	0	1	1	0	1	1.3375
0	0	0	1	1	1	0	1.3250
0	0	0	1	1	1	1	1.3125
0	0	1	0	0	0	0	1.3000
0	0	1	0	0	0	1	1.2875
0	0	1	0	0	1	0	1.2750
0	0	1	0	0	1	1	1.2625
0	0	1	0	1	0	0	1.2500
0	0	1	0	1	0	1	1.2375



Table 2. Voltage Identification Definition (Sheet 2 of 4)

VID6	VID5	VID4	VID3	VID2	VID1	VID0	V <sub>CC</sub> (V)
0	0	1	0	1	1	0	1.2250
0	0	1	0	1	1	1	1.2125
0	0	1	1	0	0	0	1.2000
0	0	1	1	0	0	1	1.1875
0	0	1	1	0	1	0	1.1750
0	0	1	1	0	1	1	1.1625
0	0	1	1	1	0	0	1.1500
0	0	1	1	1	0	1	1.1375
0	0	1	1	1	1	0	1.1250
0	0	1	1	1	1	1	1.1125
0	1	0	0	0	0	0	1.1000
0	1	0	0	0	0	1	1.0875
0	1	0	0	0	1	0	1.0750
0	1	0	0	0	1	1	1.0625
0	1	0	0	1	0	0	1.0500
0	1	0	0	1	0	1	1.0375
0	1	0	0	1	1	0	1.0250
0	1	0	0	1	1	1	1.0125
0	1	0	1	0	0	0	1.0000
0	1	0	1	0	0	1	0.9875
0	1	0	1	0	1	0	0.9750
0	1	0	1	0	1	1	0.9625
0	1	0	1	1	0	0	0.9500
0	1	0	1	1	0	1	0.9375
0	1	0	1	1	1	0	0.9250
0	1	0	1	1	1	1	0.9125
0	1	1	0	0	0	0	0.9000
0	1	1	0	0	0	1	0.8875
0	1	1	0	0	1	0	0.8750
0	1	1	0	0	1	1	0.8625
0	1	1	0	1	0	0	0.8500
0	1	1	0	1	0	1	0.8375
0	1	1	0	1	1	0	0.8250
0	1	1	0	1	1	1	0.8125
0	1	1	1	0	0	0	0.8000
0	1	1	1	0	0	1	0.7875
0	1	1	1	0	1	0	0.7750
0	1	1	1	0	1	1	0.7625
0	1	1	1	1	0	0	0.7500
0	1	1	1	1	0	1	0.7375
0	1	1	1	1	1	0	0.7250
0	1	1	1	1	1	1	0.7125
1	0	0	0	0	0	0	0.7000
1	0	0	0	0	0	1	0.6875
1	0	0	0	0	1	0	0.6750
1	0	0	0	0	1	1	0.6625
1	0	0	0	1	0	0	0.6500





Table 2. Voltage Identification Definition (Sheet 3 of 4)

VID6	VID5	VID4	VID3	VID2	VID1	VID0	V <sub>CC</sub> (V)
1	0	0	0	1	0	1	0.6375
1	0	0	0	1	1	0	0.6250
1	0	0	0	1	1	1	0.6125
1	0	0	1	0	0	0	0.6000
1	0	0	1	0	0	1	0.5875
1	0	0	1	0	1	0	0.5750
1	0	0	1	0	1	1	0.5625
1	0	0	1	1	0	0	0.5500
1	0	0	1	1	0	1	0.5375
1	0	0	1	1	1	0	0.5250
1	0	0	1	1	1	1	0.5125
1	0	1	0	0	0	0	0.5000
1	0	1	0	0	0	1	0.4875
1	0	1	0	0	1	0	0.4750
1	0	1	0	0	1	1	0.4625
1	0	1	0	1	0	0	0.4500
1	0	1	0	1	0	1	0.4375
1	0	1	0	1	1	0	0.4250
1	0	1	0	1	1	1	0.4125
1	0	1	1	0	0	0	0.4000
1	0	1	1	0	0	1	0.3875
1	0	1	1	0	1	0	0.3750
1	0	1	1	0	1	1	0.3625
1	0	1	1	1	0	0	0.3500
1	0	1	1	1	0	1	0.3375
1	0	1	1	1	1	0	0.3250
1	0	1	1	1	1	1	0.3125
1	1	0	0	0	0	0	0.3000
1	1	0	0	0	0	1	0.2875
1	1	0	0	0	1	0	0.2750
1	1	0	0	0	1	1	0.2625
1	1	0	0	1	0	0	0.2500
1	1	0	0	1	0	1	0.2375
1	1	0	0	1	1	0	0.2250
1	1	0	0	1	1	1	0.2125
1	1	0	1	0	0	0	0.2000
1	1	0	1	0	0	1	0.1875
1	1	0	1	0	1	0	0.1750
1	1	0	1	0	1	1	0.1625
1	1	0	1	1	0	0	0.1500
1	1	0	1	1	0	1	0.1375
1	1	0	1	1	1	0	0.1250
1	1	0	1	1	1	1	0.1125
1	1	1	0	0	0	0	0.1000
1	1	1	0	0	0	1	0.0875
1	1	1	0	0	1	0	0.0750
1	1	1	0	0	1	1	0.0625

Table 2. Voltage Identification Definition (Sheet 4 of 4)

VID6	VID5	VID4	VID3	VID2	VID1	VID0	V <sub>CC</sub> (V)
1	1	1	0	1	0	0	0.0500
1	1	1	0	1	0	1	0.0375
1	1	1	0	1	1	0	0.0250
1	1	1	0	1	1	1	0.0125
1	1	1	1	0	0	0	0.0000
1	1	1	1	0	0	1	0.0000
1	1	1	1	0	1	0	0.0000
1	1	1	1	0	1	1	0.0000
1	1	1	1	1	0	0	0.0000
1	1	1	1	1	0	1	0.0000
1	1	1	1	1	1	0	0.0000
1	1	1	1	1	1	1	0.0000

### 3.4 Catastrophic Thermal Protection

The processor supports the THERMTRIP# signal for catastrophic thermal protection. An external thermal sensor should also be used to protect the processor and the system against excessive temperatures. Even with the activation of THERMTRIP#, which halts all processor internal clocks and activity, leakage current can be high enough that the processor cannot be protected in all conditions without power removal to the processor. If the external thermal sensor detects a catastrophic processor temperature of 125°C (maximum), or if the THERMTRIP# signal is asserted, the V<sub>CC</sub> supply to the processor must be turned off within 500 ms to prevent permanent silicon damage due to thermal runaway of the processor. THERMTRIP# functionality is not guaranteed if the PWRGOOD signal is not asserted.

### 3.5 Reserved and Unused Pins

All RESERVED (RSVD) pins must remain unconnected. Connection of these pins to V<sub>CC</sub>, V<sub>SS</sub>, or to any other signal (including each other) may result in component malfunction or incompatibility with future processors. See [Section 4.2](#) for a pin listing of the processor and the location of all RSVD pins.

For reliable operation, always connect unused inputs or bidirectional signals to an appropriate signal level. Unused active low AGTL+ inputs may be left as no connects if AGTL+ termination is provided on the processor silicon. Unused active high inputs should be connected through a resistor to ground (V<sub>SS</sub>). Unused outputs can be left unconnected.

The TEST1 and TEST2 pins must have a stuffing option of separate pull-down resistors to V<sub>SS</sub>.

For the purpose of testability, route the TEST3 and TEST5 signals through a ground-referenced Zo = 55-Ω trace that ends in a via that is near a GND via and is accessible through an oscilloscope connection.



## 3.6 FSB Frequency Select Signals (BSEL[2:0])

The BSEL[2:0] signals are used to select the frequency of the processor input clock (BCLK[1:0]). These signals should be connected to the clock chip and the appropriate chipset on the platform. The BSEL encoding for BCLK[1:0] is shown in [Table 3](#).

**Table 3. BSEL[2:0] Encoding for BCLK Frequency**

BSEL[2]	BSEL[1]	BSEL[0]	BCLK Frequency
L	L	L	RESERVED
L	L	H	133 MHz
L	H	H	RESERVED
L	H	L	200 MHz
H	H	L	RESERVED
H	H	H	RESERVED
H	L	H	RESERVED
H	L	L	RESERVED

## 3.7 FSB Signal Groups

The FSB signals have been combined into groups by buffer type in the following sections. AGTL+ input signals have differential input buffers, which use GTLREF as a reference level. In this document, the term “AGTL+ Input” refers to the AGTL+ input group as well as the AGTL+ I/O group when receiving. Similarly, “AGTL+ Output” refers to the AGTL+ output group as well as the AGTL+ I/O group when driving.

With the implementation of a source synchronous data bus, two sets of timing parameters need to be specified. One set is for common clock signals, which are dependent upon the rising edge of BCLK0 (ADS#, HIT#, HITM#, etc.) and the second set is for the source synchronous signals, which are relative to their respective strobe lines (data and address) as well as the rising edge of BCLK0. Asynchronous signals are still present (A20M#, IGNNE#, etc.) and can become active at any time during the clock cycle. [Table 4](#) identifies which signals are common clock, source synchronous, and asynchronous.

Table 4. FSB Pin Groups

Signal Group	Type	Signals <sup>1</sup>														
AGTL+ Common Clock Input	Synchronous to BCLK[1:0]	BPRI#, DEFER#, PREQ# <sup>5</sup> , RESET#, RS[2:0]#, TRDY#														
AGTL+ Common Clock I/O	Synchronous to BCLK[1:0]	ADS#, BNR#, BPM[3:0]# <sup>3</sup> , BR0#, DBSY#, DRDY#, HIT#, HITM#, LOCK#, PRDY# <sup>3</sup> , DPWR#														
AGTL+ Source Synchronous I/O	Synchronous to assoc. strobe	<table><tr><th>Signals</th><th>Associated Strobe</th></tr><tr><td>REQ[4:0]#, A[16:3]#</td><td>ADSTB[0]#</td></tr><tr><td>A[35:17]#</td><td>ADSTB[1]#</td></tr><tr><td>D[15:0]#, DINV0#</td><td>DSTBP0#, DSTBN0#</td></tr><tr><td>D[31:16]#, DINV1#</td><td>DSTBP1#, DSTBN1#</td></tr><tr><td>D[47:32]#, DINV2#</td><td>DSTBP2#, DSTBN2#</td></tr><tr><td>D[63:48]#, DINV3#</td><td>DSTBP3#, DSTBN3#</td></tr></table>	Signals	Associated Strobe	REQ[4:0]#, A[16:3]#	ADSTB[0]#	A[35:17]#	ADSTB[1]#	D[15:0]#, DINV0#	DSTBP0#, DSTBN0#	D[31:16]#, DINV1#	DSTBP1#, DSTBN1#	D[47:32]#, DINV2#	DSTBP2#, DSTBN2#	D[63:48]#, DINV3#	DSTBP3#, DSTBN3#
Signals	Associated Strobe															
REQ[4:0]#, A[16:3]#	ADSTB[0]#															
A[35:17]#	ADSTB[1]#															
D[15:0]#, DINV0#	DSTBP0#, DSTBN0#															
D[31:16]#, DINV1#	DSTBP1#, DSTBN1#															
D[47:32]#, DINV2#	DSTBP2#, DSTBN2#															
D[63:48]#, DINV3#	DSTBP3#, DSTBN3#															
AGTL+ Strobes	Synchronous to BCLK[1:0]	ADSTB[1:0]#, DSTBP[3:0]#, DSTBN[3:0]#														
CMOS Input	Asynchronous	A20M#, DPRSTP#, DPSLP#, IGNNE#, INIT#, LINT0/INTR, LINT1/NMI, PWRGOOD, SMI#, SLP#, STPCLK#														
Open Drain Output	Asynchronous	FERR#, IERR#, THERMTRIP#														
Open Drain I/O	Asynchronous	PROCHOT# <sup>4</sup>														
CMOS Output	Asynchronous	PSI#, VID[6:0], BSEL[2:0]														
CMOS Input	Synchronous to TCK	TCK, TDI, TMS, TRST#														
Open Drain Output	Synchronous to TCK	TDO														
FSB Clock	Clock	BCLK[1:0]														
Power/Other		COMP[3:0], DBR# <sup>2</sup> , GTLREF, RSVD, TEST2, TEST1, THERMDA, THERMDC, V <sub>CC</sub> , V <sub>CCA</sub> , V <sub>CCP</sub> , V <sub>CC_SENSE</sub> , V <sub>SS</sub> , V <sub>SS_SENSE</sub>														

**NOTES:**

1. Refer to Chapter 4 for signal descriptions and termination requirements.
2. In processor systems where there is no debug port implemented on the system board, these signals are used to support a debug port interposer. In systems with the debug port implemented on the system board, these signals are no connects.
3. BPM[2:1]# and PRDY# are AGTL+ output only signals.
4. PROCHOT# signal type is open drain output and CMOS input.
5. On die termination differs from other AGTL+ signals.



## 3.8 CMOS Signals

CMOS input signals are shown in [Table 4](#). Legacy output FERR#, IERR# and other non-AGTL+ signals (THERMTRIP# and PROCHOT#) utilize Open Drain output buffers. These signals do not have setup or hold time specifications in relation to BCLK[1:0]. However, all of the CMOS signals are required to be asserted for more than four BCLKs in order for the processor to recognize them. See [Section 3.10](#) for the DC specifications for the CMOS signal groups.

## 3.9 Maximum Ratings

[Table 5](#) specifies absolute maximum and minimum ratings. If the processor stays within functional operation limits, functionality and long-term reliability can be expected.

**Caution:** At conditions outside functional operation condition limits, but within absolute maximum and minimum ratings, neither functionality nor long term reliability can be expected. At conditions exceeding absolute maximum and minimum ratings, neither functionality nor long term reliability can be expected.

**Caution:** Precautions should always be taken to avoid high static voltages or electric fields.

**Table 5. Processor Absolute Maximum Ratings**

Symbol	Parameter	Min	Max	Unit	Notes <sup>1</sup>
T <sub>STORAGE</sub>	Processor storage temperature	-40	85	°C	2, 3, 4
V <sub>CC</sub>	Any processor supply voltage with respect to V <sub>SS</sub>	-0.3	1.55	V	
V <sub>InAGTL+</sub>	AGTL+ buffer DC input voltage with respect to V <sub>SS</sub>	-0.1	1.55	V	
V <sub>InAsynch_CMOS</sub>	CMOS buffer DC input voltage with respect to V <sub>SS</sub>	-0.1	1.55	V	

**NOTES:**

1. For functional operation, all processor electrical, signal quality, mechanical and thermal specifications must be satisfied.
2. Storage temperature is applicable to storage conditions only. In this scenario, the processor must not receive a clock, and no lands can be connected to a voltage bias. Storage within these limits does not affect the long term reliability of the device. For functional operation, please refer to the processor case temperature specifications.
3. This rating applies to the processor and does not include any tray or packaging.
4. Failure to adhere to this specification can affect the long term reliability of the processor.

### 3.10 Processor DC Specifications

The processor DC specifications in this section are defined at the processor core (pads) unless noted otherwise. See Table 4 for the pin signal definitions and signal pin assignments.

Table 6 through Table 8 list the DC specifications for the processor and are valid only while meeting specifications for junction temperature, clock frequency, and input voltages. The Highest Frequency Mode (HFM) and Super Low Frequency Mode (SuperLFM) refer to the highest and lowest core operating frequencies supported on the processor. Active mode load line specifications apply in all states except in the Deep Sleep and Deeper Sleep states.  $V_{CC,BOOT}$  is the default voltage driven by the voltage regulator at power up in order to set the VID values. Unless specified otherwise, all specifications for the processor are at  $T_{junction} = 100^{\circ}C$ . Care should be taken to read all notes associated with each parameter.

**Table 6. Voltage and Current Specifications for the Intel Core 2 Duo Processors - Standard Voltage (Sheet 1 of 2)**

Symbol	Parameter		Min	Typ	Max	Unit	Notes
$V_{CCDAM}$	$V_{CC}$ in Intel® Dynamic Acceleration Technology Mode		1.0375		1.3500	V	1, 2
$V_{CCHFM}$	$V_{CC}$ at High Frequency Mode (HFM)		1.0375		1.3000	V	1, 2
$V_{CCLFM}$	$V_{CC}$ at Low Frequency Mode (LFM)		0.8500		1.0500	V	1, 2, 8
$V_{CCSLFM}$	$V_{CC}$ at Super Low Frequency Mode (SuperLFM)		0.7500		0.9500	V	1, 2
$V_{CC,BOOT}$	Default $V_{CC}$ Voltage for Initial Power Up			1.20		V	2
$V_{CCP}$	AGTL+ Termination Voltage		1.00	1.05	1.10	V	
$V_{CCA}$	PLL Supply Voltage		1.425	1.5	1.575	V	
$V_{CCDPRSLP}$	$V_{CC}$ at Deeper Sleep		0.6000		0.8000	V	1, 2
$V_{CCDC4}$	$V_{CC}$ at Intel® Enhanced Deeper Sleep Voltage		0.5500		0.7500	V	1, 2, 8
$I_{CCDES}$	Standard Voltage Processor $I_{CC}$ Recommended Design Target				44	A	6
$I_{CC}$	Standard Voltage $I_{CC}$ for the Processor						
	Processor Number	Core Frequency/Voltage					
	T7800	2.6 GHz & $V_{CCHFM}$			41	A	3, 4, 5, 12, 13
	T7700	2.4 GHz & $V_{CCHFM}$			41		3, 4, 5, 12, 13
	T7500	2.2 GHz & $V_{CCHFM}$			41		3, 4, 5, 12, 13
	T7300	2.0 GHz & $V_{CCHFM}$			41		3, 4, 5, 12, 13
	T7250	2.0 GHz & $V_{CCHFM}$			41		3, 4, 5, 12, 14
	T7100	1.8 GHz & $V_{CCHFM}$			41		
		1.2 GHz & $V_{CCLFM}$			30.1		
		0.8 GHz & $V_{CCSLFM}$			25.5		
$I_{AH}, I_{SGNT}$	$I_{CC}$ Auto-Halt & Stop-Grant HFM SuperLFM				27.9 17.0	A	3, 4, 12
$I_{SLP}$	$I_{CC}$ Sleep HFM SuperLFM				27.4 16.8	A	3, 4, 12


**Table 6. Voltage and Current Specifications for the Intel Core 2 Duo Processors - Standard Voltage (Sheet 2 of 2)**

Symbol	Parameter	Min	Typ	Max	Unit	Notes
$I_{\text{DSL P}}$	$I_{\text{CC}}$ Deep Sleep HFM SuperLFM			25.0 16.0	A	3, 4, 12
$I_{\text{DPRSLP}}$	$I_{\text{CC}}$ Deeper Sleep			11.5	A	3, 4
$I_{\text{DC4}}$	$I_{\text{CC}}$ Intel Enhanced Deeper Sleep			9.4	A	3, 4
$di_{\text{CC/DT}}$	$V_{\text{CC}}$ Power Supply Current Slew Rate at Processor Package Pin			600	A/ $\mu$ s	7, 9
$I_{\text{CCA}}$	$I_{\text{CC}}$ for $V_{\text{CCA}}$ Supply			130	mA	
$I_{\text{CCP}}$	$I_{\text{CC}}$ for $V_{\text{CCP}}$ Supply before $V_{\text{CC}}$ Stable			4.5	A	10
	$I_{\text{CC}}$ for $V_{\text{CCP}}$ Supply after $V_{\text{CC}}$ Stable			2.5	A	11

**NOTES:**

- Each processor is programmed with a maximum valid voltage identification value (VID), which is set at manufacturing and cannot be altered. Individual maximum VID values are calibrated during manufacturing in such a way that two processors at the same frequency may have different settings within the VID range. Note that this differs from the VID employed by the processor during a power management event (Intel Thermal Monitor 2, Enhanced Intel SpeedStep Technology, or Extended Halt State).
- The voltage specifications are assumed to be measured across  $V_{\text{CC\_SENSE}}$  and  $V_{\text{SS\_SENSE}}$  pins at socket with a 100-MHz bandwidth oscilloscope, 1.5-pF maximum probe capacitance, and 1-m $\Omega$  minimum impedance. The maximum length of ground wire on the probe should be less than 5 mm. Ensure external noise from the system is not coupled in the scope probe.
- Specified at 100°C Tj.
- Specified at the nominal  $V_{\text{CC}}$ .
- 800-MHz FSB supported
- Instantaneous current  $I_{\text{CC\_CORE\_INST}}$  of 55 A has to be sustained for short time ( $t_{\text{INST}}$ ) of 10  $\mu$ s. Average current is less than maximum specified  $I_{\text{CCDES}}$ . VR OCP threshold should be high enough to support current levels described herein.
- Measured at the bulk capacitors on the motherboard.
- The maximum delta between Intel Enhanced Deeper Sleep and LFM on the processor is lesser than or equal to 350 mV.
- Based on simulations and averaged over the duration of any change in current. Specified by design/characterization at nominal  $V_{\text{CC}}$ . Not 100% tested.
- This is a power-up peak current specification, which is applicable when  $V_{\text{CCP}}$  is high and  $V_{\text{CC\_CORE}}$  is low.
- This is a steady-state  $I_{\text{CC}}$  current specification, which is applicable when both  $V_{\text{CCP}}$  and  $V_{\text{CC\_CORE}}$  are high.
- Processor  $I_{\text{CC}}$  requirements in Intel Dynamic Acceleration Technology mode is lesser than  $I_{\text{CC}}$  in HFM.
- 4-M L2 cache.
- 2-M L2 cache.



**Table 7. Voltage and Current Specifications for the Intel Core 2 Duo Processors - Low Voltage**

Symbol	Parameter		Min	Typ	Max	Unit	Notes
V <sub>CCDAM</sub>	V <sub>CC</sub> in Intel® Dynamic Acceleration Technology Mode		0.9000		1.3000	V	1, 2
V <sub>CCHFM</sub>	V <sub>CC</sub> at High Frequency Mode (HFM)		0.9000		1.2000	V	1, 2
V <sub>CCLFM</sub>	V <sub>CC</sub> at Low Frequency Mode (LFM)		0.9000		1.0500	V	1, 2, 13
V <sub>CCSLFM</sub>	V <sub>CC</sub> at Super Low Frequency Mode (SuperLFM)		0.7500		0.9500	V	1, 2
V <sub>CC,BOOT</sub>	Default V <sub>CC</sub> Voltage for Initial Power Up			1.20		V	2
V <sub>CCP</sub>	AGTL+ Termination Voltage		1.00	1.05	1.10	V	
V <sub>CCA</sub>	PLL Supply Voltage		1.425	1.5	1.575	V	
V <sub>CCDPRSLP</sub>	V <sub>CC</sub> at Deeper Sleep		0.6000		0.8000	V	1, 2
V <sub>CCDC4</sub>	V <sub>CC</sub> at Intel® Enhanced Deeper Sleep Voltage		0.5500		0.7000	V	1, 2, 13
I <sub>CCDES</sub>	Low Voltage Processor I <sub>CC</sub> Recommended Design Target				23	A	6
I <sub>CC</sub>	Low Voltage I <sub>CC</sub> for the Processor						
	Processor Number	Core Frequency/Voltage					
	L7700	1.8 GHz & V <sub>CCHFM</sub>			23	A	3, 4, 5, 8, 12
	L7500	1.6 GHz & V <sub>CCHFM</sub>			23		
L7300		1.4 GHz & V <sub>CCHFM</sub>			23		
		1.2 GHz & V <sub>CCLFM</sub>			21		
I <sub>AH</sub> , I <sub>SGNT</sub>	I <sub>CC</sub> Auto-Halt & Stop-Grant						
	HFM SuperLFM				11.7 8.3	A	3, 4, 12
I <sub>SLP</sub>	I <sub>CC</sub> Sleep						
	HFM SuperLFM				11.4 8.1	A	3, 4, 12
I <sub>DSP</sub>	I <sub>CC</sub> Deep Sleep						
	HFM SuperLFM				10.0 7.3	A	3, 4, 12
I <sub>DPRSLP</sub>	I <sub>CC</sub> Deeper Sleep				6.3	A	3, 4
I <sub>DC4</sub>	I <sub>CC</sub> Intel Enhanced Deeper Sleep				4.7	A	3, 4
dI <sub>CC</sub> /DT	V <sub>CC</sub> Power Supply Current Slew Rate at Processor Package Pin				600	A/μs	7, 9
I <sub>CCA</sub>	I <sub>CC</sub> for V <sub>CCA</sub> Supply				130	mA	
I <sub>CCP</sub>	I <sub>CC</sub> for V <sub>CCP</sub> Supply before V <sub>CC</sub> Stable				4.5	A	10
	I <sub>CC</sub> for V <sub>CCP</sub> Supply after V <sub>CC</sub> Stable				2.5	A	11

**NOTES:**

- Each processor is programmed with a maximum valid voltage identification value (VID), which is set at manufacturing and cannot be altered. Individual maximum VID values are calibrated during manufacturing such that two processors at the same frequency may have different settings within the VID range. Note that this differs from the VID employed by the processor during a power management event (Intel Thermal Monitor 2, Enhanced Intel SpeedStep Technology, or Enhanced Halt State).





2. The voltage specifications are assumed to be measured across  $V_{CC\_SENSE}$  and  $V_{SS\_SENSE}$  pins at socket with a 100-MHz bandwidth oscilloscope, 1.5-pF maximum probe capacitance, and 1-m $\Omega$  minimum impedance. The maximum length of ground wire on the probe should be less than 5 mm. Ensure external noise from the system is not coupled in the scope probe.
3. Specified at 100°C Tj.
4. Specified at the nominal  $V_{CC}$ .
5. 800-MHz FSB supported.
6. Instantaneous current  $I_{CC\_CORE\_INST}$  of 30 A has to be sustained for short time ( $t_{INST}$ ) of 10  $\mu$ s. Average current is less than maximum specified  $I_{CCDES}$ . VR OCP threshold should be high enough to support current levels described herein.
7. Measured at the bulk capacitors on the motherboard.
8. 4-M L2 cache.
9. Based on simulations and averaged over the duration of any change in current. Specified by design/characterization at nominal  $V_{CC}$ . Not 100% tested.
10. This is a power-up peak current specification, which is applicable when  $V_{CCP}$  is high and  $V_{CC\_CORE}$  is low.
11. This is a steady-state  $I_{CC}$  current specification, which is applicable when both  $V_{CCP}$  and  $V_{CC\_CORE}$  are high.
12. Processor  $I_{CC}$  requirements in Intel Dynamic Acceleration Technology mode is lesser than  $I_{CC}$  in HFM.
13. The maximum delta between Intel Enhanced Deeper Sleep and LFM on the processor is lesser than or equal to 350 mV.

**Table 8. Voltage and Current Specifications for the Intel Core 2 Duo -Ultra Low Voltage Processors (Sheet 1 of 2)**

Symbol	Parameter		Min	Typ	Max	Unit	Notes
$V_{CCDAM}$	$V_{CC}$ in Intel® Dynamic Acceleration Mode		0.8000		1.2000	V	1, 2
$V_{CCHFM}$	$V_{CC}$ at High Frequency Mode (HFM)		0.8000		0.9750	V	1, 2
$V_{CCLFM}$	$V_{CC}$ at Low Frequency Mode (LFM)		0.7500		0.9500	V	1, 2, 13
$V_{CC,BOOT}$	Default $V_{CC}$ Voltage for Initial Power Up			1.20		V	2
$V_{CCP}$	AGTL+ Termination Voltage		1.00	1.05	1.10	V	
$V_{CCA}$	PLL Supply Voltage		1.425	1.5	1.575	V	
$V_{CCDPRSLP}$	$V_{CC}$ at Deeper Sleep		0.6000		0.8000	V	1, 2
$V_{CCDC4}$	$V_{CC}$ at Intel® Enhanced Deeper Sleep voltage		0.5500		0.7500	V	1, 2, 13
$I_{CCDES}$	Ultra Low Voltage Processor $I_{CC}$ Recommended Design Target				17	A	6
$I_{CC}$	Ultra Low Voltage $I_{CC}$ for the Processor						
	Processor Number	Core Frequency/Voltage					
	U7700	1.33 GHz & $V_{CCHFM}$			16	A	3, 4, 5, 8, 12, 14
	U7600	1.20 GHz & $V_{CCHFM}$			16		
	U7500	1.06 GHz & $V_{CCHFM}$			16		
		0.80 GHz & $V_{CCLFM}$			13.8		
$I_{AH}, I_{SGNT}$	$I_{CC}$ Auto-Halt & Stop-Grant HFM LFM				7.4 6.5	A	3, 4, 12
$I_{SLP}$	$I_{CC}$ Sleep HFM LFM				7.2 6.3	A	3, 4, 12
$I_{DPLP}$	$I_{CC}$ Deep Sleep HFM LFM				6.2 5.7	A	3, 4, 12
$I_{DPRSLP}$	$I_{CC}$ Deeper Sleep				4.9	A	3, 4



**Table 8. Voltage and Current Specifications for the Intel Core 2 Duo -Ultra Low Voltage Processors (Sheet 2 of 2)**

Symbol	Parameter	Min	Typ	Max	Unit	Notes
$I_{DC4}$	$I_{CC}$ Intel Enhanced Deeper Sleep			4.0	A	3, 4
$dI_{CC}/DT$	$V_{CC}$ Power Supply Current Slew Rate at Processor Package Pin			600	A/ $\mu$ s	7, 9
$I_{CCA}$	$I_{CC}$ for $V_{CCA}$ Supply			130	mA	
$I_{CCP}$	$I_{CC}$ for $V_{CCP}$ Supply before $V_{CC}$ Stable			4.5	A	10
	$I_{CC}$ for $V_{CCP}$ Supply after $V_{CC}$ Stable			2.5	A	11

**NOTES:**

- Each processor is programmed with a maximum valid voltage identification value (VID), which is set at manufacturing and cannot be altered. Individual maximum VID values are calibrated during manufacturing such that two processors at the same frequency may have different settings within the VID range. Note that this differs from the VID employed by the processor during a power management event (Intel Thermal Monitor 2, Enhanced Intel SpeedStep Technology, or Enhanced Halt State).
- The voltage specifications are assumed to be measured across  $V_{CC\_SENSE}$  and  $V_{SS\_SENSE}$  pins at socket with a 100-MHz bandwidth oscilloscope, 1.5-pF maximum probe capacitance, and 1-m $\Omega$  minimum impedance. The maximum length of ground wire on the probe should be less than 5 mm. Ensure external noise from the system is not coupled in the scope probe.
- Specified at 100°C Tj.
- Specified at the nominal  $V_{CC}$ .
- 533-MHz FSB supported.
- Instantaneous current  $I_{CC\_CORE\_INST}$  of 21 A has to be sustained for short time ( $t_{INST}$ ) of 10  $\mu$ s. Average current is less than maximum specified  $I_{CCDES}$ . VR OCP threshold should be high enough to support current levels described herein.
- Measured at the bulk capacitors on the motherboard.
- 2-M L2 cache.
- Based on simulations and averaged over the duration of any change in current. Specified by design/characterization at nominal  $V_{CC}$ . Not 100% tested.
- This is a power-up peak current specification, which is applicable when  $V_{CCP}$  is high and  $V_{CC\_CORE}$  is low.
- This is a steady-state  $I_{CC}$  current specification, which is applicable when both  $V_{CCP}$  and  $V_{CC\_CORE}$  are high.
- Processor  $I_{CC}$  requirements in Intel Dynamic Acceleration Technology mode is lesser than  $I_{CC}$  in HFM.
- The maximum delta between Intel Enhanced Deeper Sleep and LFM on the processor is lesser than or equal to 350 mV.
- Dynamic FSB Frequency Switching not supported.

**Table 9. Voltage and Current Specifications for the Intel Core 2 Extreme Processors (Sheet 1 of 2)**

Symbol	Parameter	Min	Typ	Max	Unit	Notes
$V_{CCHFM}$	$V_{CC}$ at High Frequency Mode (HFM)	1.1000		1.3750	V	1, 2
$V_{CCLFM}$	$V_{CC}$ at Low Frequency Mode (LFM)	1.0000		1.1000	V	1, 2, 7
$V_{CCSLFM}$	$V_{CC}$ at Super Low Frequency Mode (SuperLFM)	0.9000		1.1000	V	1, 2
$V_{CC\_BOOT}$	Default $V_{CC}$ Voltage for Initial Power Up		1.20		V	2
$V_{CCP}$	AGTL+ Termination Voltage	1.00	1.05	1.10	V	
$V_{CCA}$	PLL Supply Voltage	1.425	1.5	1.575	V	
$V_{CCDPRSLP}$	$V_{CC}$ at Deeper Sleep	0.7000		0.9000	V	1, 2
$V_{CCDC4}$	$V_{CC}$ at Intel® Enhanced Deeper Sleep Voltage	0.6500		0.8500	V	1, 2, 7
$I_{CCDES}$	Extreme Processor $I_{CC}$ Recommended Design Target			55	A	

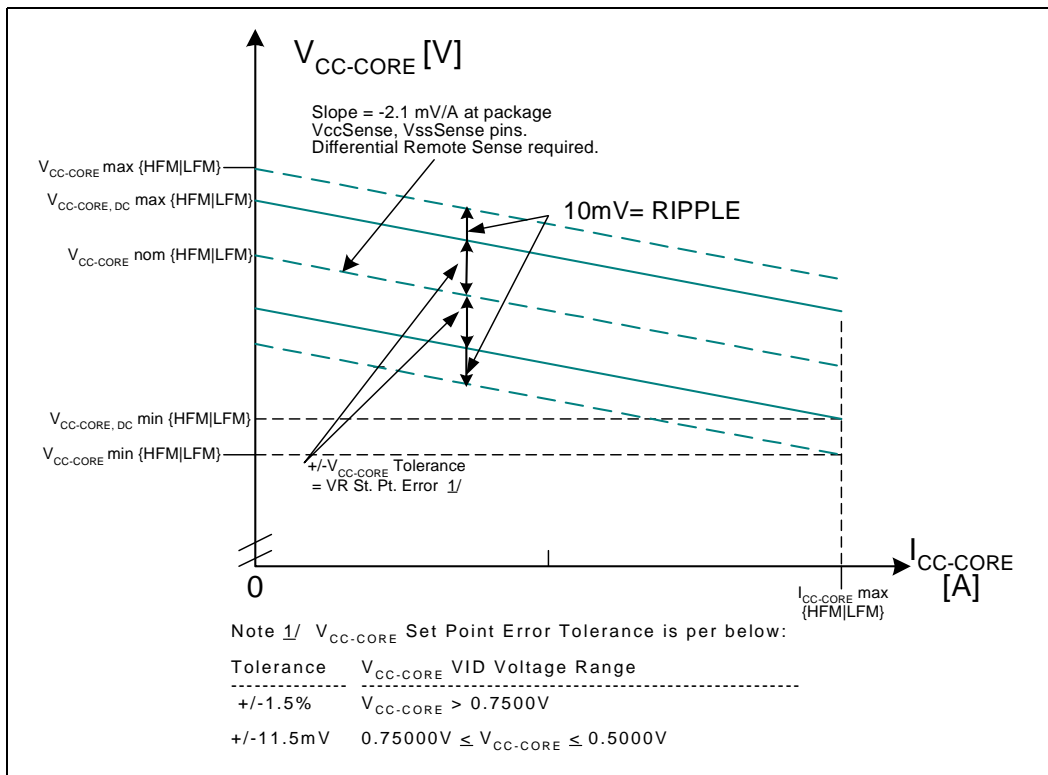

**Table 9. Voltage and Current Specifications for the Intel Core 2 Extreme Processors (Sheet 2 of 2)**

Symbol	Parameter		Min	Typ	Max	Unit	Notes
$I_{CC}$	Extreme Processor $I_{CC}$ for the Processor						
	Processor Number	Core Frequency/Voltage					
	X7900	2.80 GHz & $V_{CCHFM}$			55	A	3, 4, 5, 11, 12
	X7800	2.60 GHz & $V_{CCHFM}$			55		
		1.20 GHz & $V_{CCLFM}$			37		
		0.80 GHz & $V_{CCSLFM}$			29		
$I_{AH}$ , $I_{SGNT}$	$I_{CC}$ Auto-Halt & Stop-Grant HFM SuperLFM				29.8 21.6	A	3, 4
$I_{SLP}$	$I_{CC}$ Sleep HFM SuperLFM				29.1 21.4	A	3, 4
$I_{DSLP}$	$I_{CC}$ Deep Sleep HFM SuperLFM				26.6 20.6	A	3, 4
$I_{DPRSLP}$	$I_{CC}$ Deeper Sleep				14.7	A	3, 4
$I_{DC4}$	$I_{CC}$ Intel Enhanced Deeper Sleep				13.5	A	3, 4
$dI_{CC}/DT$	$V_{CC}$ Power Supply Current Slew Rate at Processor Package Pin				600	A/ $\mu$ s	6, 8
$I_{CCA}$	$I_{CC}$ for $V_{CCA}$ Supply				130	mA	
$I_{CCP}$	$I_{CC}$ for $V_{CCP}$ Supply before $V_{CC}$ Stable				4.5	A	9
	$I_{CC}$ for $V_{CCP}$ Supply after $V_{CC}$ Stable				2.5	A	10

**NOTES:**

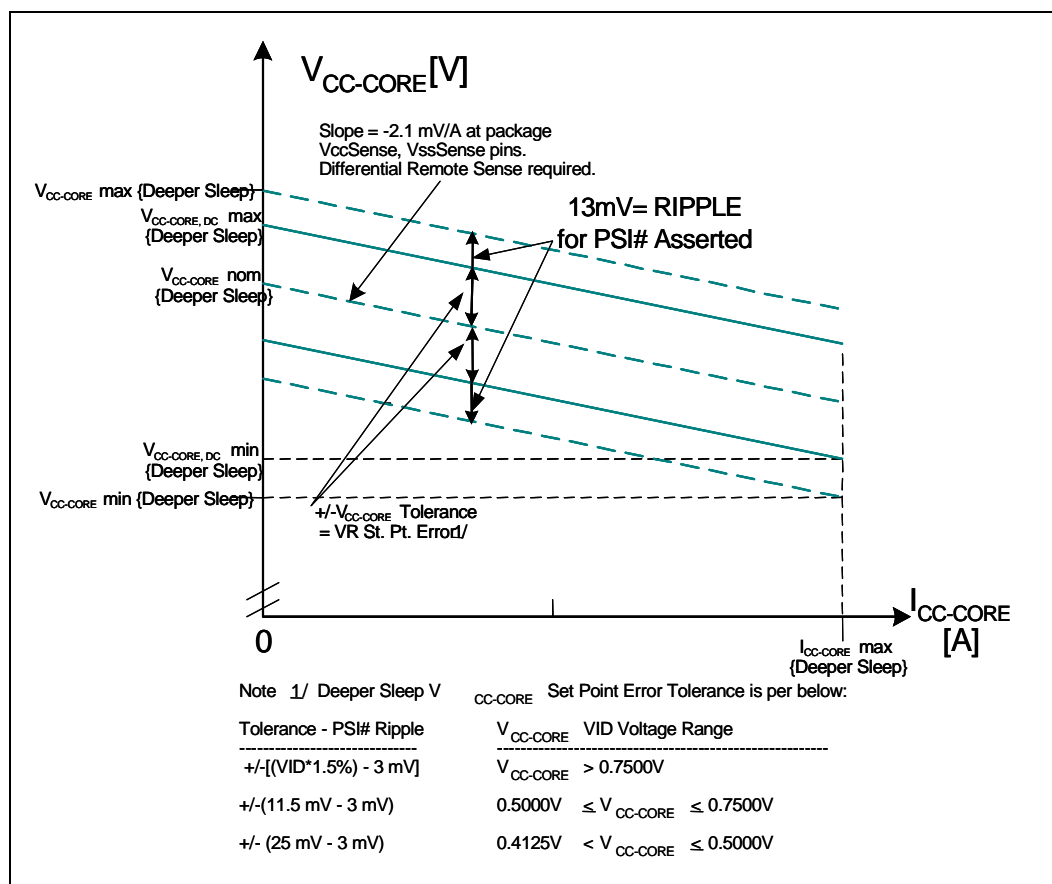
- Each processor is programmed with a maximum valid voltage identification value (VID), which is set at manufacturing and cannot be altered. Individual maximum VID values are calibrated during manufacturing such that two processors at the same frequency may have different settings within the VID range. Note that this differs from the VID employed by the processor during a power management event (Intel Thermal Monitor 2, Enhanced Intel SpeedStep Technology, or Enhanced Halt State).
- The voltage specifications are assumed to be measured across  $V_{CC\_SENSE}$  and  $V_{SS\_SENSE}$  pins at socket with a 100-MHz bandwidth oscilloscope, 1.5-pF maximum probe capacitance, and 1-m $\Omega$  minimum impedance. The maximum length of ground wire on the probe should be less than 5 mm. Ensure external noise from the system is not coupled in the scope probe.
- Specified at 100°C Tj.
- Specified at the nominal  $V_{CC}$ .
- 800-MHz FSB Supported
- Measured at the bulk capacitors on the motherboard.
- The maximum delta between Intel Enhanced Deeper Sleep and LFM on the processor is lesser than or equal to 350 mV.
- Based on simulations and averaged over the duration of any change in current. Specified by design/characterization at nominal  $V_{CC}$ . Not 100% tested.
- This is a power-up peak current specification, which is applicable when  $V_{CCP}$  is high and  $V_{CC\_CORE}$  is low.
- This is a steady-state  $I_{CC}$  current specification, which is applicable when both  $V_{CCP}$  and  $V_{CC\_CORE}$  are high.
- 4-M L2 cache.
- Intel Dynamic Acceleration Technology not supported.

**Figure 3. Active  $V_{CC}$  and  $I_{CC}$  Loadline Intel Core 2 Duo Processors - Standard Voltage, Low Voltage and Ultra Low Voltage and Intel Core 2 Extreme Processors (PSI# Not Asserted)**



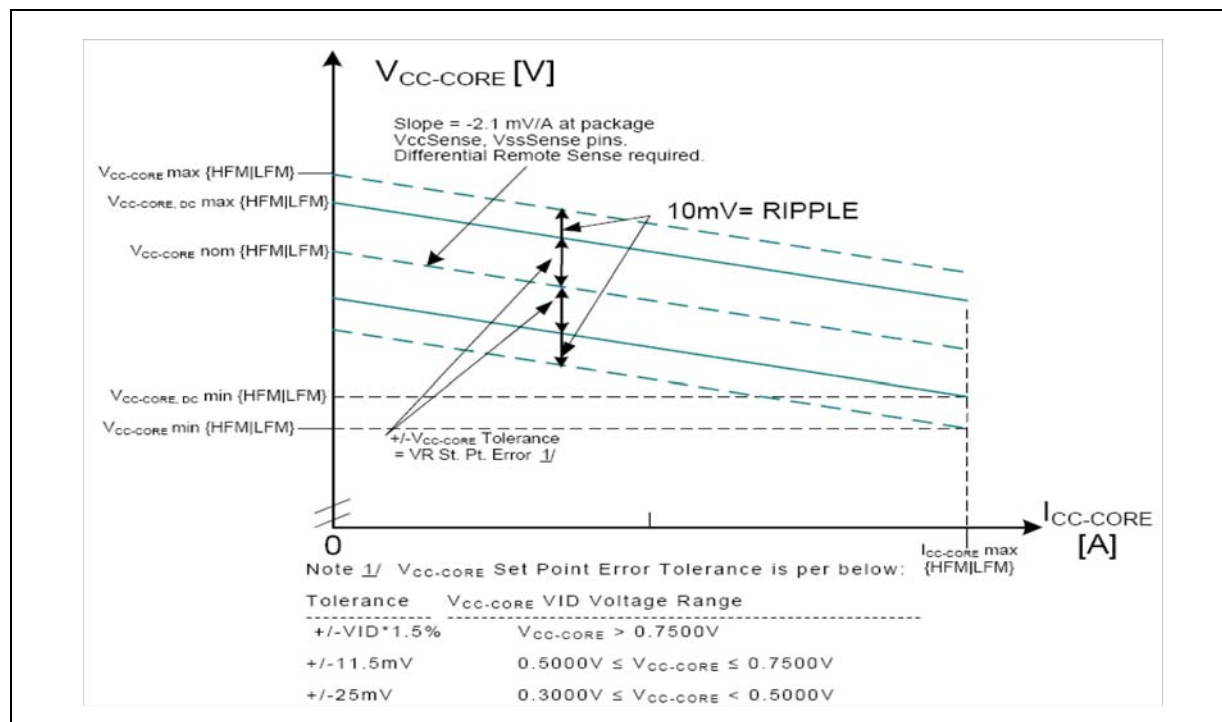


**Figure 4. Deeper Sleep  $V_{CC}$  and  $I_{CC}$  Loadline Intel Core 2 Duo Processors - Standard Voltage and Intel Core 2 Extreme Processors (PSI# Asserted)**



**NOTE:** Deeper Sleep mode tolerance depends on VID value.

**Figure 5. Deeper Sleep  $V_{CC}$  and  $I_{CC}$  Loadline Intel Core 2 Duo Processor - Low Voltage and Ultra Low Voltage (PSI# Asserted)**



**NOTE:** Deeper Sleep mode tolerance depends on VID value.

**Table 10. FSB Differential BCLK Specifications**

Symbol	Parameter	Min	Typ	Max	Unit	Notes <sup>1</sup>
$V_{CROSS}$	Crossing Voltage	0.3		0.55	V	2, 7, 8
$\Delta V_{CROSS}$	Range of Crossing Points			140	mV	2, 7, 5
$V_{SWING}$	Differential Output Swing	300			mV	6
$I_{LI}$	Input Leakage Current	-5		+5	$\mu A$	3
Cpad	Pad Capacitance	0.95	1.2	1.45	pF	4

**NOTES:**

1. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
2. Crossing Voltage is defined as absolute voltage where rising edge of BCLK0 is equal to the falling edge of BCLK1.
3. For  $V_{in}$  between 0 V and  $V_{IH}$ .
4. Cpad includes die capacitance only. No package parasitics are included.
5.  $\Delta V_{CROSS}$  is defined as the total variation of all crossing voltages as defined in Note 2.
6. Measurement taken from differential waveform.
7. Measurement taken from single-ended waveform.
8. Only applies to the differential rising edge (Clock rising and Clock# falling).



Table 11. AGTL+ Signal Group DC Specifications

Symbol	Parameter	Min	Typ	Max	Unit	Notes <sup>1</sup>
V <sub>CCP</sub>	I/O Voltage	1.00	1.05	1.10	V	
GTLREF	Reference Voltage		2/3 V <sub>CCP</sub>		V	6
R <sub>COMP</sub>	Compensation Resistor	27.23	27.5	27.78	Ω	10
R <sub>ODT</sub>	Termination Resistor		55		Ω	11
V <sub>IH</sub>	Input High Voltage	GTLREF+0.10	V <sub>CCP</sub>	V <sub>CCP</sub> +0.10	V	3,6
V <sub>IL</sub>	Input Low Voltage	-0.10	0	GTLREF-0.10	V	2,4
V <sub>OH</sub>	Output High Voltage	V <sub>CCP</sub> -0.10	V <sub>CCP</sub>	V <sub>CCP</sub>		6
R <sub>TT</sub>	Termination Resistance	50	55	61	Ω	7
R <sub>ON</sub>	Buffer On Resistance	22	25	28	Ω	5
I <sub>LI</sub>	Input Leakage Current			±100	μA	8
Cpad	Pad Capacitance	1.6	2.1	2.55	pF	9

**NOTES:**

1. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
2. V<sub>IL</sub> is defined as the maximum voltage level at a receiving agent that is interpreted as a logical low value.
3. V<sub>IH</sub> is defined as the minimum voltage level at a receiving agent that is interpreted as a logical high value.
4. V<sub>IH</sub> and V<sub>OH</sub> may experience excursions above V<sub>CCP</sub>. However, input signal drivers must comply with the signal quality specifications.
5. This is the pull-down driver resistance. Measured at 0.31\*V<sub>CCP</sub>. R<sub>ON</sub> (min) = 0.4\*R<sub>TT</sub>, R<sub>ON</sub> (typ) = 0.455\*R<sub>TT</sub>, R<sub>ON</sub> (max) = 0.51\*R<sub>TT</sub>. R<sub>TT</sub> typical value of 55 Ω is used for R<sub>ON</sub> typ/min/max calculations.
6. GTLREF should be generated from V<sub>CCP</sub> with a 1%-tolerance resistor divider. The V<sub>CCP</sub> referred to in these specifications is the instantaneous V<sub>CCP</sub>.
7. R<sub>TT</sub> is the on-die termination resistance measured at V<sub>OL</sub> of the AGTL+ output driver. Measured at 0.31\*V<sub>CCP</sub>. R<sub>TT</sub> is connected to V<sub>CCP</sub> on die.
8. Specified with on die R<sub>TT</sub> and R<sub>ON</sub> turned off. Vin between 0 and V<sub>CCP</sub>.
9. Cpad includes die capacitance only. No package parasitics are included.
10. This is the external resistor on the comp pins.
11. On die termination resistance measured at 0.33\*V<sub>CCP</sub>.

Table 12. CMOS Signal Group DC Specifications

Symbol	Parameter	Min	Typ	Max	Unit	Notes <sup>1</sup>
V <sub>CCP</sub>	I/O Voltage	1.00	1.05	1.10	V	
V <sub>IH</sub>	Input High Voltage	0.7*V <sub>CCP</sub>	V <sub>CCP</sub>	V <sub>CCP</sub> +0.1	V	2
V <sub>IL</sub>	Input Low Voltage CMOS	-0.10	0.00	0.3*V <sub>CCP</sub>	V	2
V <sub>OH</sub>	Output High Voltage	0.9*V <sub>CCP</sub>	V <sub>CCP</sub>	V <sub>CCP</sub> +0.1	V	2
V <sub>OL</sub>	Output Low Voltage	-0.10	0	0.1*V <sub>CCP</sub>	V	2
I <sub>OH</sub>	Output High Current	1.5		4.1	mA	5
I <sub>OL</sub>	Output Low Current	1.5		4.1	mA	4
I <sub>LI</sub>	Input Leakage Current			±100	µA	6
Cpad1	Pad Capacitance	1.6	2.1	2.55	pF	7
Cpad2	Pad Capacitance for CMOS Input	0.95	1.2	1.45		3

**NOTES:**

1. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
2. The V<sub>CCP</sub> referred to in these specifications refers to instantaneous V<sub>CCP</sub>.
3. Cpad2 includes die capacitance for all other CMOS input signals. No package parasitics are included.
4. Measured at 0.1\*V<sub>CCP</sub>.
5. Measured at 0.9\*V<sub>CCP</sub>.
6. For Vin between 0 V and V<sub>CCP</sub>. Measured when the driver is tristated.
7. Cpad1 includes die capacitance only for DPRSTP#, DPSLP#, PWRGOOD. No package parasitics are included.

Table 13. Open Drain Signal Group DC Specifications

Symbol	Parameter	Min	Typ	Max	Unit	Notes <sup>1</sup>
V <sub>OH</sub>	Output High Voltage	V <sub>CCP</sub> -5%	V <sub>CCP</sub>	V <sub>CCP</sub> +5%	V	3
V <sub>OL</sub>	Output Low Voltage	0		0.20	V	
I <sub>OL</sub>	Output Low Current	16		50	mA	2
I <sub>LO</sub>	Output Leakage Current			±200	µA	4
Cpad	Pad Capacitance	1.9	2.2	2.45	pF	5

**NOTES:**

1. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
2. Measured at 0.2 V.
3. V<sub>OH</sub> is determined by value of the external pull-up resistor to V<sub>CCP</sub>.
4. For Vin between 0 V and V<sub>OH</sub>.
5. Cpad includes die capacitance only. No package parasitics are included.





## 4 Package Mechanical Specifications and Pin Information

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### 4.1 Package Mechanical Specifications

The processor is available in 4-MB and 2-MB, 478-pin Micro-FCPGA packages as well as 4-MB and 2-MB, 479-ball Micro-FCBGA packages. The package mechanical dimensions, keep-out zones, processor mass specifications, and package loading specifications are shown in [Figure 6](#) through [Figure 13](#).

The mechanical package pressure specifications are in a direction normal to the surface of the processor. This requirement is to protect the processor die from fracture risk due to uneven die pressure distribution under tilt, stack-up tolerances and other similar conditions. These specifications assume that a mechanical attach is designed specifically to load one type of processor.

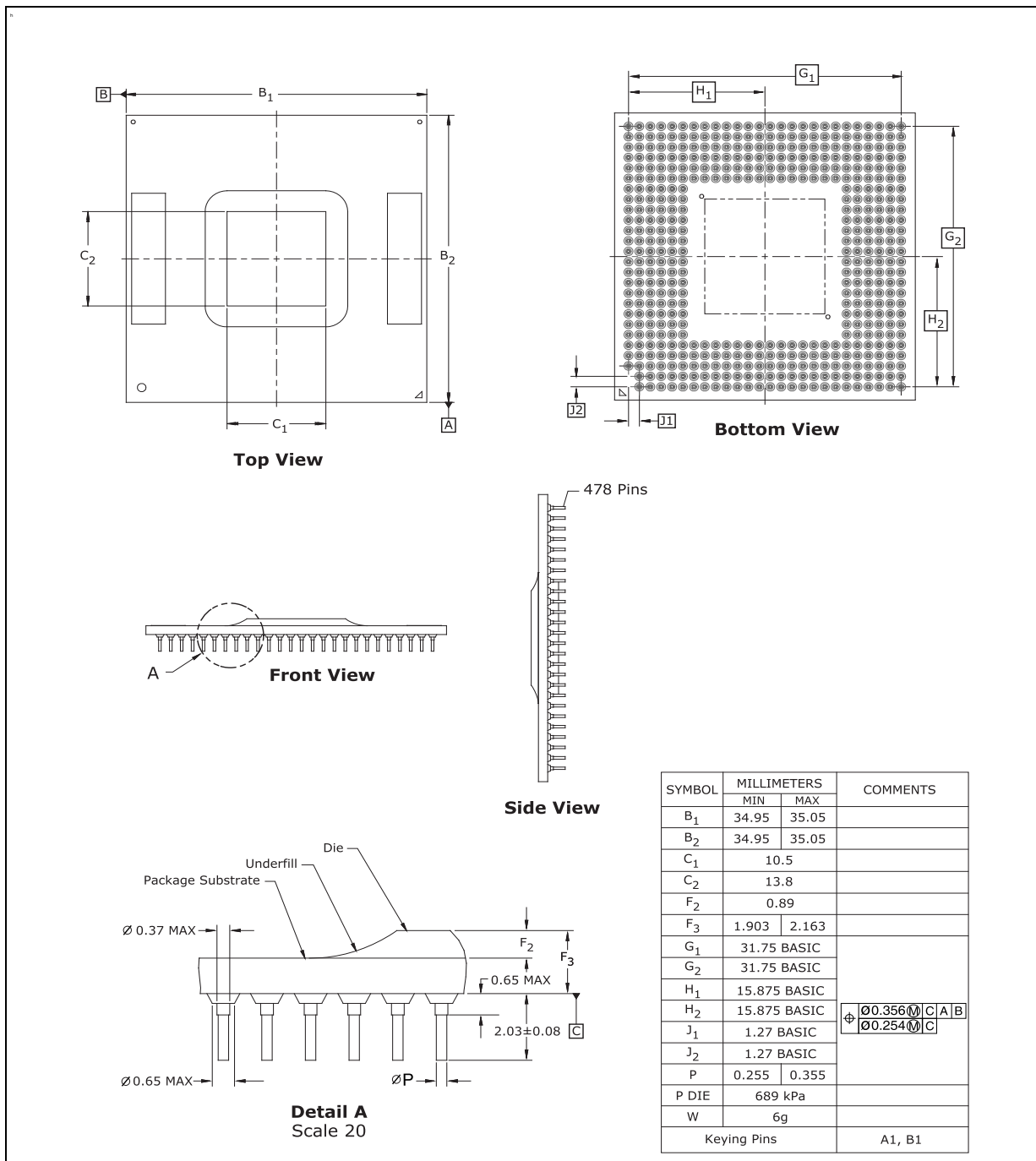
Intel also specifies that 15-lbf load limit should not be exceeded on any of Intel's BGA packages so as to not impact solder joint reliability after reflow. This load limit ensures that impact to the package solder joints due to transient bend, shock, or tensile loading is minimized. The 15-lbf metric should be used **in parallel** with the 689-kPa (100 psi) pressure limit as long as neither limits are exceeded.

Moreover, the processor package substrate should not be used as a mechanical reference or load-bearing surface for the thermal or mechanical solution. Please refer to the *Santa Rosa Platform Mechanical Design Guide* for more details.

**Caution:** The Micro-FCBGA package incorporates land-side capacitors. The land-side capacitors are electrically conductive so care should be taken to avoid contacting the capacitors with other electrically conductive materials on the motherboard. Doing so may short the capacitors and possibly damage the device or render it inactive.

**Note:** For E-step based processors refer the 4-MB and Fused 2-MB package drawings. For M-step based processors refer to the 2-MB package drawings.

Figure 6. 4-MB and Fused 2-MB Micro-FCPGA Processor Package Drawing (Sheet 1 of 2)



**Figure 7. 4-MB and Fused 2-MB Micro-FCPGA Processor Package Drawing (Sheet 2 of 2)**

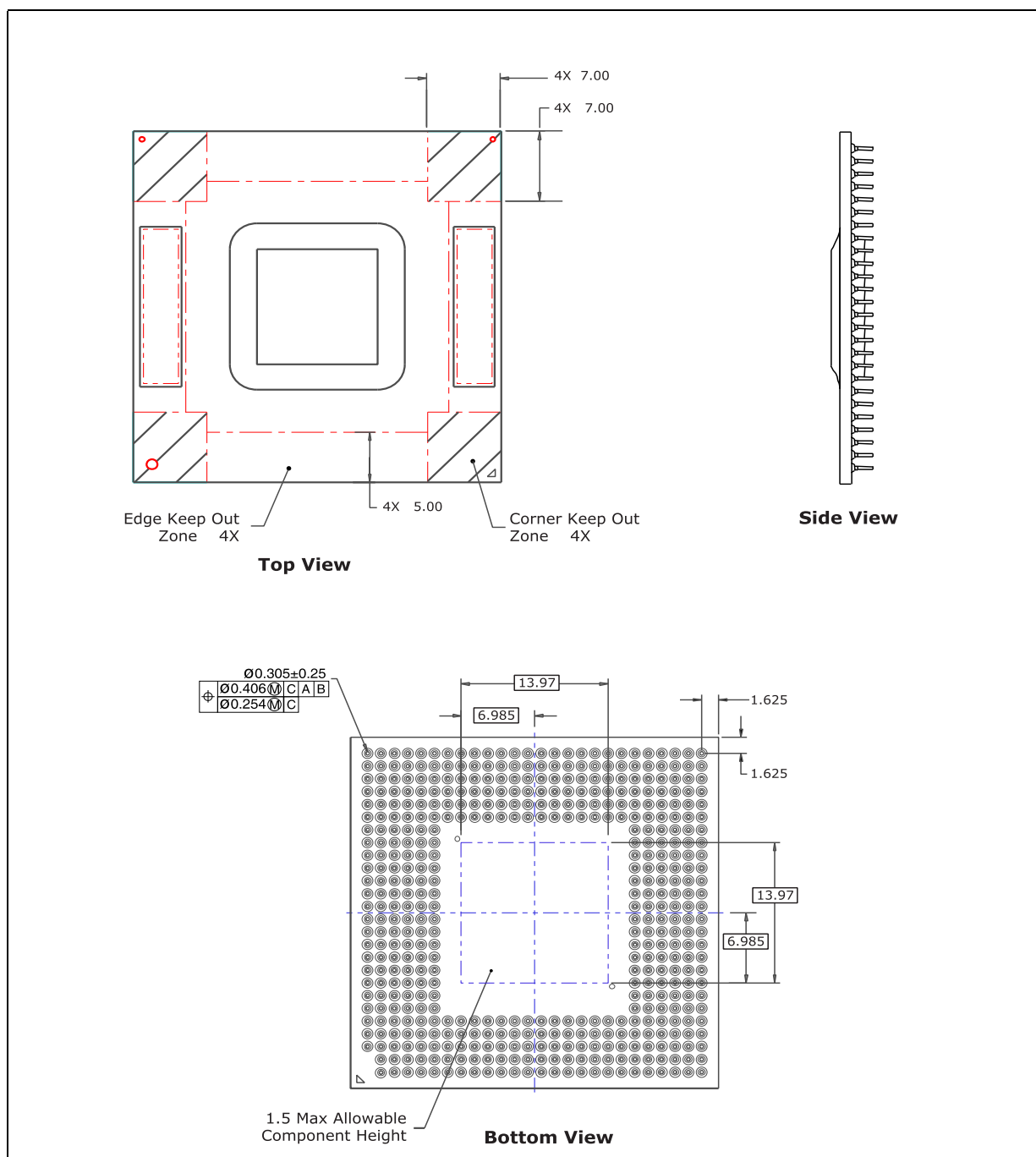


Figure 8. 2-MB Micro-FCPGA Processor Package Drawing (Sheet 1 of 2)

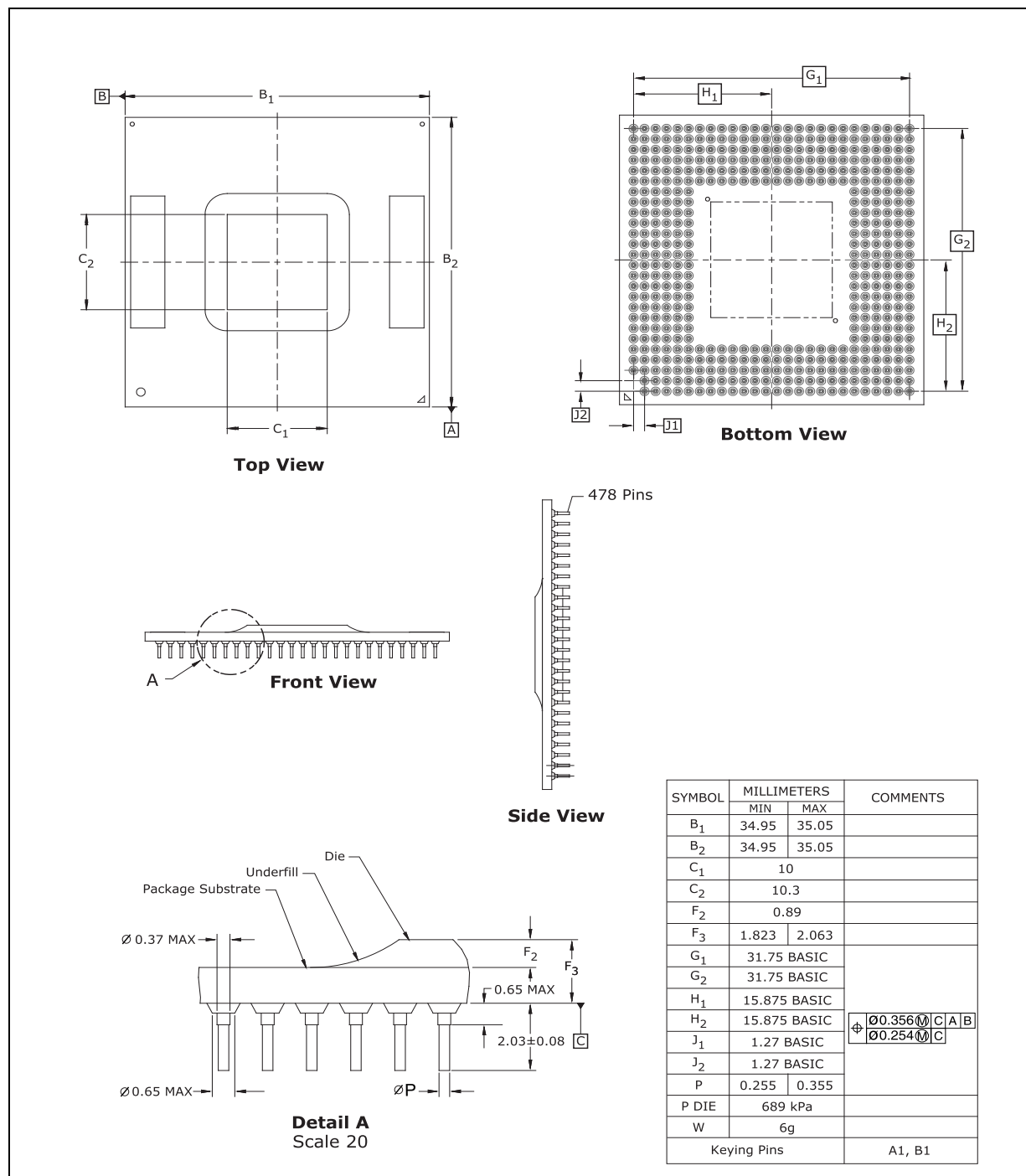


Figure 9. 2-MB Micro-FCPGA Processor Package Drawing (Sheet 2 of 2)

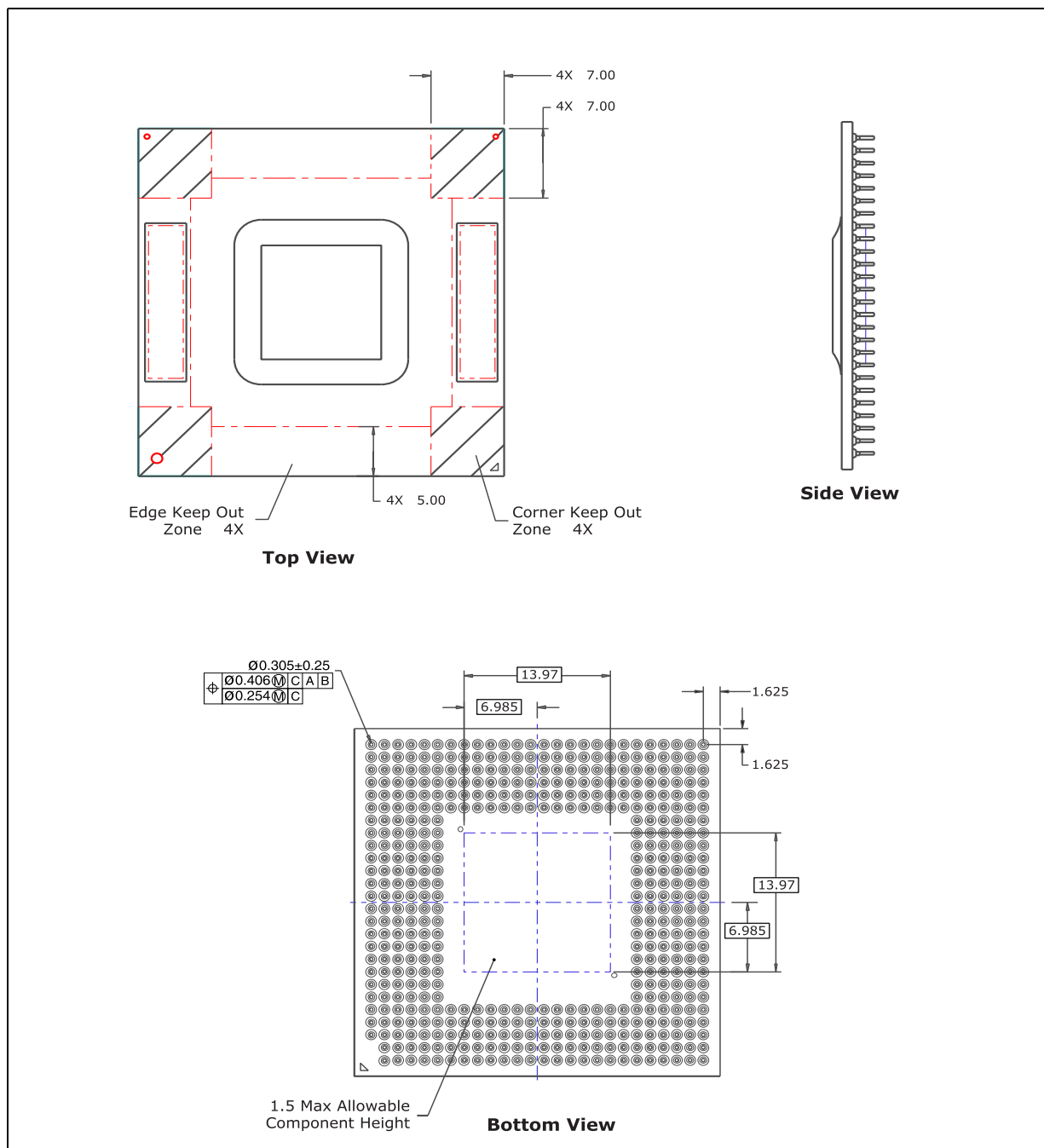


Figure 10. 4-MB and Fused 2-MB Micro-FCBGA Processor Package Drawing (Sheet 1 of 2)

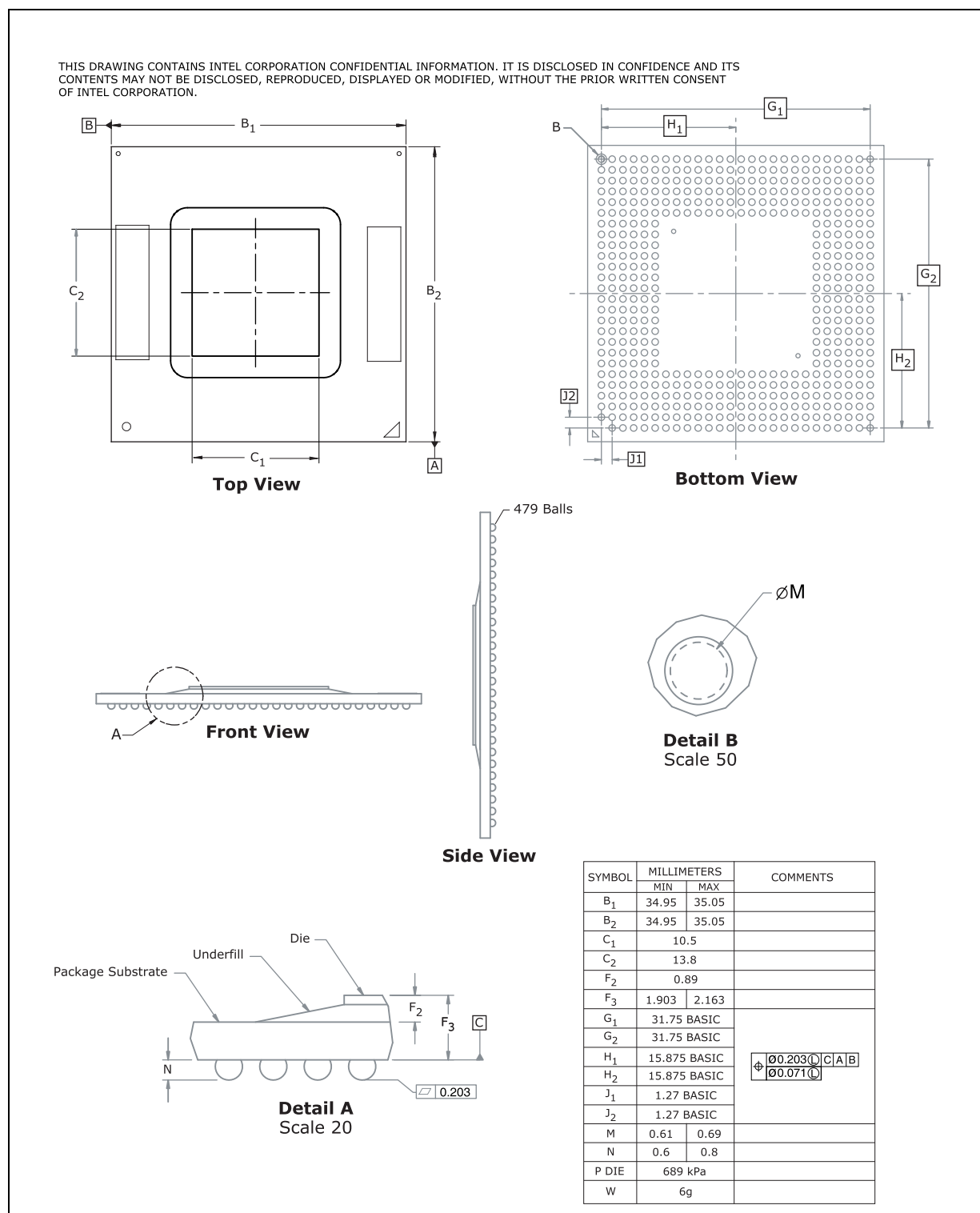




Figure 11. 4-MB and Fused 2-MB Micro-FCBGA Processor Package Drawing (Sheet 2 of 2)

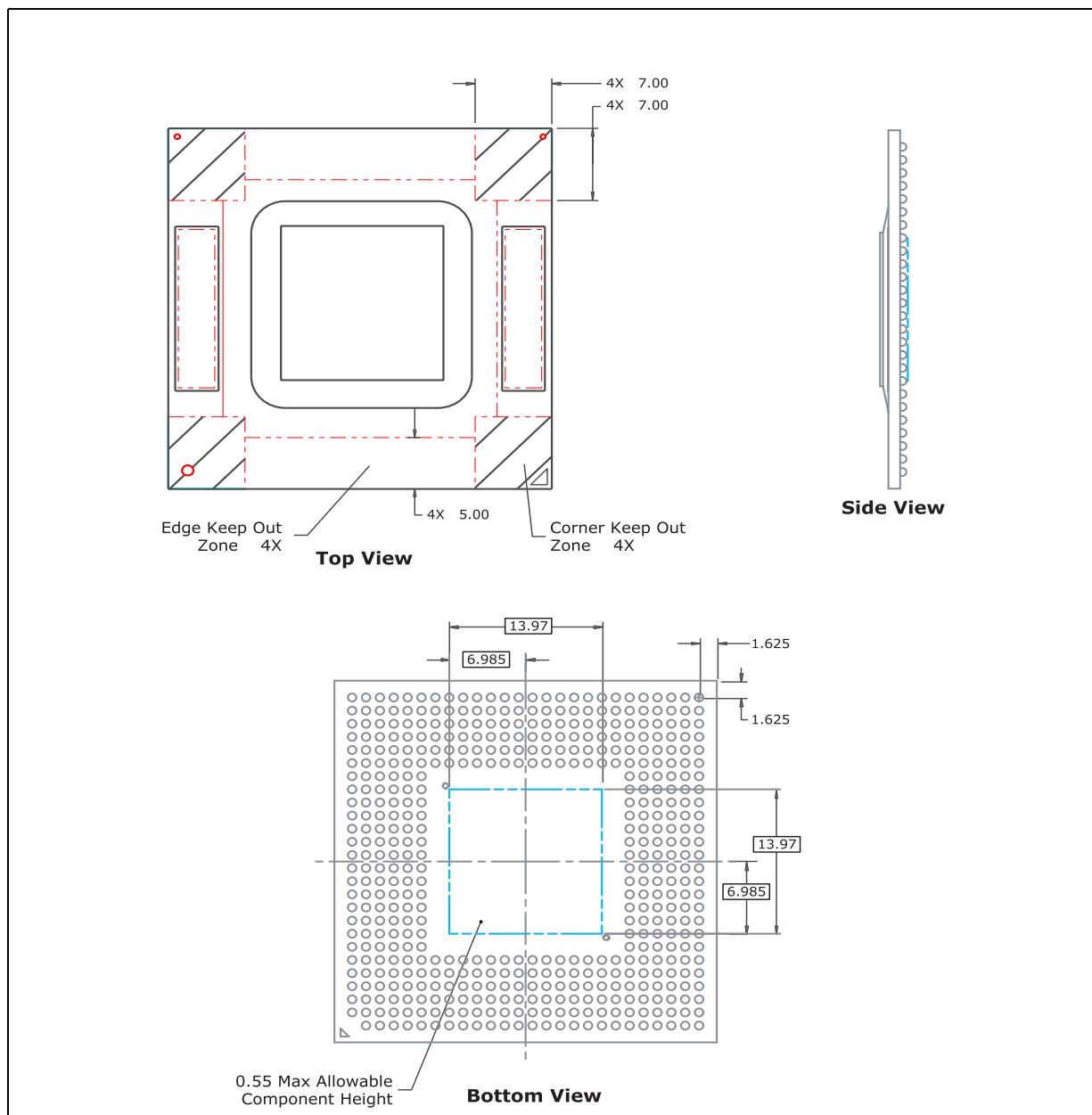


Figure 12. 2-MB Micro-FCBGA Processor Package Drawing (Sheet 1 of 2)

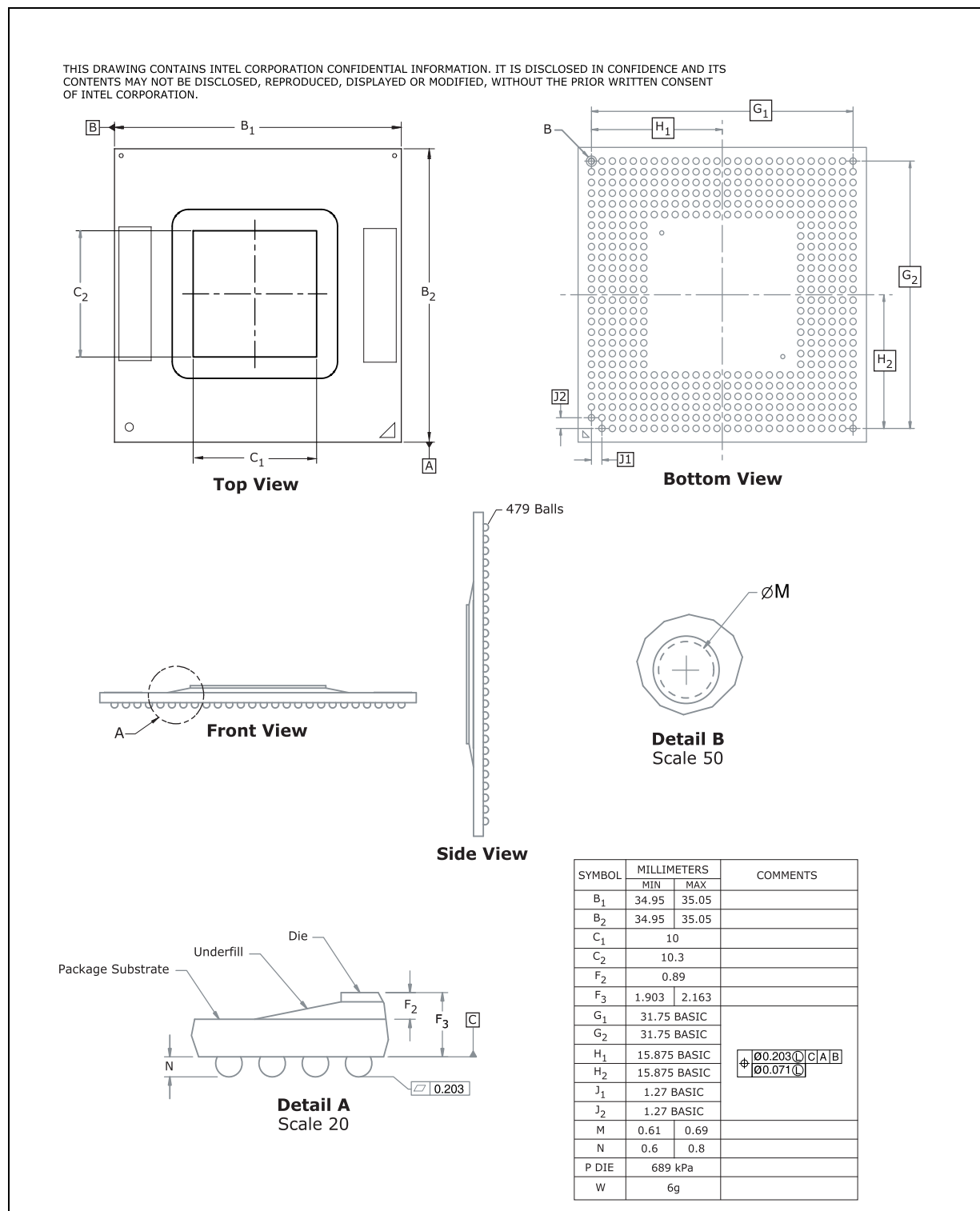
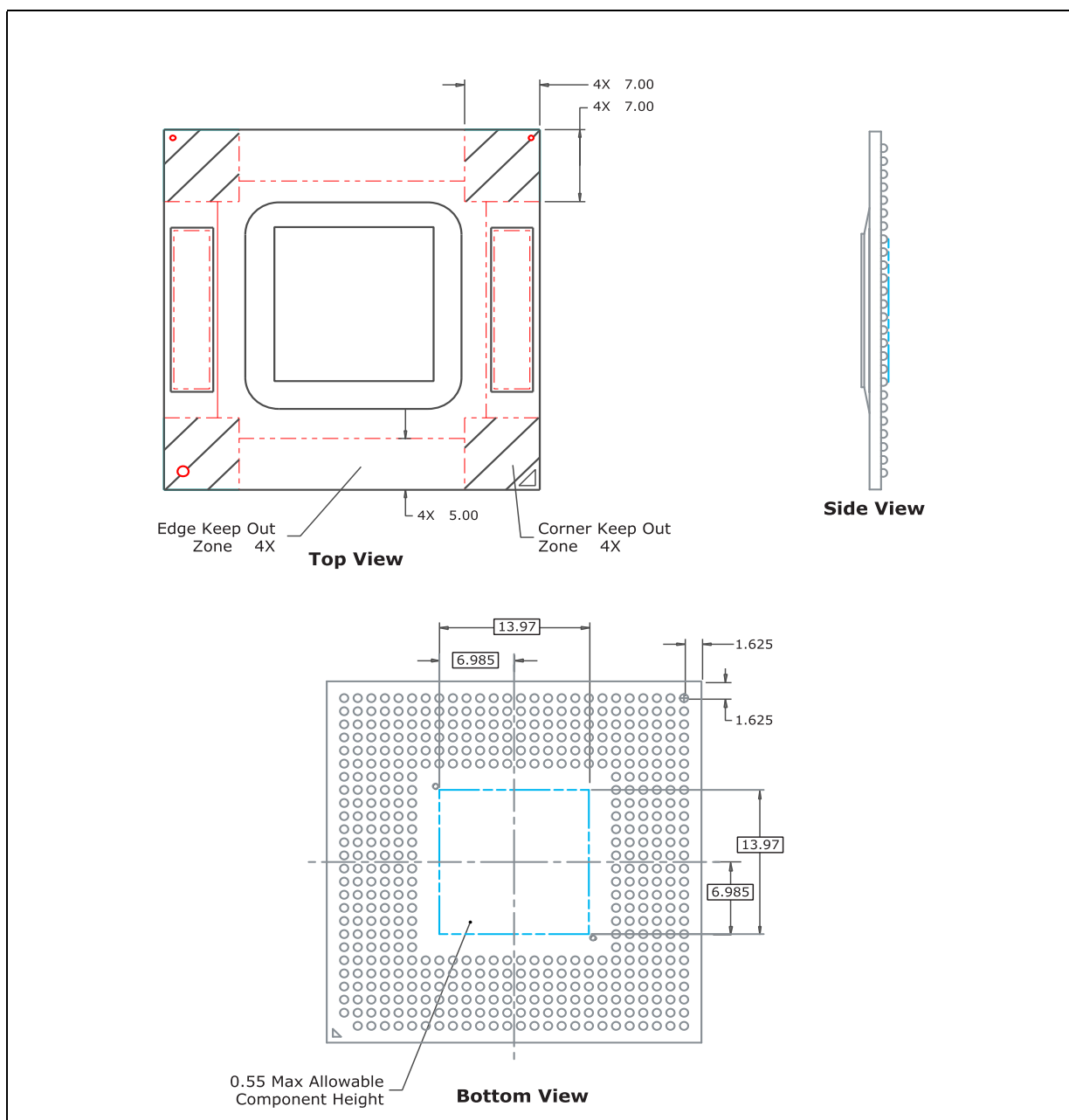




Figure 13. 2-MB Micro-FCBGA Processor Package Drawing (Sheet 2 of 2)



## 4.2 Processor Pinout and Pin List

Table 14 shows the top view pinout of the Intel Core 2 Duo mobile processor. The pin list, arranged in two different formats, is shown in the following pages.



**Table 14. The Coordinates of the Processor Pins as Viewed from the Top of the Package (Sheet 1 of 2)**

	1	2	3	4	5	6	7	8	9	10	11	12	13	
<b>A</b>		VSS	SMI#	VSS	FERR#	A20M#	VCC	VSS	VCC	VCC	VSS	VCC	VCC	<b>A</b>
<b>B</b>		RSVD	INIT#	LINT1	DPSLP#	VSS	VCC	VSS	VCC	VCC	VSS	VCC	VSS	<b>B</b>
<b>C</b>	RESET#	VSS	RSVD	IGNNE#	VSS	LINT0	THERM TRIP#	VSS	VCC	VCC	VSS	VCC	VCC	<b>C</b>
<b>D</b>	VSS	RSVD	RSVD	VSS	STPCLK#	PWRGOD	SLP#	VSS	VCC	VCC	VSS	VCC	VSS	<b>D</b>
<b>E</b>	DBSY#	BNR#	VSS	HITM#	DPRSTP#	VSS	VCC	VSS	VCC	VCC	VSS	VCC	VCC	<b>E</b>
<b>F</b>	BR0#	VSS	RS[0]#	RS[1]#	VSS	RSVD	VCC	VSS	VCC	VCC	VSS	VCC	VSS	<b>F</b>
<b>G</b>	VSS	TRDY#	RS[2]#	VSS	BPRI#	HIT#								<b>G</b>
<b>H</b>	ADS#	REQ[1]#	VSS	LOCK#	DEFER#	VSS								<b>H</b>
<b>J</b>	A[9]#	VSS	REQ[3]#	A[3]#	VSS	VCCP								<b>J</b>
<b>K</b>	VSS	REQ[2]#	REQ[0]#	VSS	A[6]#	VCCP								<b>K</b>
<b>L</b>	REQ[4]#	A[13]#	VSS	A[5]#	A[4]#	VSS								<b>L</b>
<b>M</b>	ADSTB[0]#	VSS	A[7]#	RSVD	VSS	VCCP								<b>M</b>
<b>N</b>	VSS	A[8]#	A[10]#	VSS	RSVD	VCCP								<b>N</b>
<b>P</b>	A[15]#	A[12]#	VSS	A[14]#	A[11]#	VSS								<b>P</b>
<b>R</b>	A[16]#	VSS	A[19]#	A[24]#	VSS	VCCP								<b>R</b>
<b>T</b>	VSS	RSVD	A[26]#	VSS	A[25]#	VCCP								<b>T</b>
<b>U</b>	A[23]#	A[30]#	VSS	A[21]#	A[18]#	VSS								<b>U</b>
<b>V</b>	ADSTB[1]#	VSS	RSVD	A[31]#	VSS	VCCP								<b>V</b>
<b>W</b>	VSS	A[27]#	A[32]#	VSS	A[28]#	A[20]#								<b>W</b>
<b>Y</b>	COMP[3]	A[17]#	VSS	A[29]#	A[22]#	VSS								<b>Y</b>
<b>AA</b>	COMP[2]	VSS	A[35]#	A[33]#	VSS	TDI	VCC	VSS	VCC	VCC	VSS	VCC	VCC	<b>AA</b>
<b>AB</b>	VSS	A[34]#	TDO	VSS	TMS	TRST#	VCC	VSS	VCC	VCC	VSS	VCC	VSS	<b>AB</b>
<b>AC</b>	PREQ#	PRDY#	VSS	BPM[3]#	TCK	VSS	VCC	VSS	VCC	VCC	VSS	VCC	VCC	<b>AC</b>
<b>AD</b>	BPM[2]#	VSS	BPM[1]#	BPM[0]#	VSS	VID[0]	VCC	VSS	VCC	VCC	VSS	VCC	VSS	<b>AD</b>
<b>AE</b>	VSS	VID[6]	VID[4]	VSS	VID[2]	PSI#	VSS SENSE	VSS	VCC	VCC	VSS	VCC	VCC	<b>AE</b>
<b>AF</b>	TEST5	VSS	VID[5]	VID[3]	VID[1]	VSS	VCC SENSE	VSS	VCC	VCC	VSS	VCC	VSS	<b>AF</b>
	1	2	3	4	5	6	7	8	9	10	11	12	13	



**Table 15. The Coordinates of the Processor Pins as Viewed from the Top of the Package (Sheet 2 of 2)**

	14	15	16	17	18	19	20	21	22	23	24	25	26	
A	VSS	VCC	VSS	VCC	VCC	VSS	VCC	BCLK[1]	BCLK[0]	VSS	THRMDA	VSS	TEST6	A
B	VCC	VCC	VSS	VCC	VCC	VSS	VCC	VSS	BSEL[0]	BSEL[1]	VSS	THRMDC	VCCA	B
C	VSS	VCC	VSS	VCC	VCC	VSS	DBR#	BSEL[2]	VSS	TEST1	TEST3	VSS	VCCA	C
D	VCC	VCC	VSS	VCC	VCC	VSS	IERR#	PROCHOT#	RSVD	VSS	DPWR#	TEST2	VSS	D
E	VSS	VCC	VSS	VCC	VCC	VSS	VCC	VSS	D[0]#	D[7]#	VSS	D[6]#	D[2]#	E
F	VCC	VCC	VSS	VCC	VCC	VSS	VCC	DRDY#	VSS	D[4]#	D[1]#	VSS	D[13]#	F
G								VCCP	D[3]#	VSS	D[9]#	D[5]#	VSS	G
H								VSS	D[12]#	D[15]#	VSS	DINV[0]#	DSTBP[0]#	H
J								VCCP	VSS	D[11]#	D[10]#	VSS	DSTBN[0]#	J
K								VCCP	D[14]#	VSS	D[8]#	D[17]#	VSS	K
L								VSS	D[22]#	D[20]#	VSS	D[29]#	DSTBN[1]#	L
M								VCCP	VSS	D[23]#	D[21]#	VSS	DSTBP[1]#	M
N								VCCP	D[16]#	VSS	DINV[1]#	D[31]#	VSS	N
P								VSS	D[26]#	D[25]#	VSS	D[24]#	D[18]#	P
R								VCCP	VSS	D[19]#	D[28]#	VSS	COMP[0]	R
T								VCCP	D[37]#	VSS	D[27]#	D[30]#	VSS	T
U								VSS	DINV[2]#	D[39]#	VSS	D[38]#	COMP[1]	U
V								VCCP	VSS	D[36]#	D[34]#	VSS	D[35]#	V
W								VCCP	D[41]#	VSS	D[43]#	D[44]#	VSS	W
Y								VSS	D[32]#	D[42]#	VSS	D[40]#	DSTBN[2]#	Y
AA	VSS	VCC	VSS	VCC	VCC	VSS	VCC	D[50]#	VSS	D[45]#	D[46]#	VSS	DSTBP[2]#	AA
AB	VCC	VCC	VSS	VCC	VCC	VSS	VCC	D[52]#	D[51]#	VSS	D[33]#	D[47]#	VSS	AB
AC	VSS	VCC	VSS	VCC	VCC	VSS	DINV[3]#	VSS	D[60]#	D[63]#	VSS	D[57]#	D[53]#	AC
AD	VCC	VCC	VSS	VCC	VCC	VSS	D[54]#	D[59]#	VSS	D[61]#	D[49]#	VSS	GTLREF	AD
AE	VSS	VCC	VSS	VCC	VCC	VSS	VCC	D[58]#	D[55]#	VSS	D[48]#	DSTBN[3]#	VSS	AE
AF	VCC	VCC	VSS	VCC	VCC	VSS	VCC	VSS	D[62]#	D[56]#	DSTBP[3]#	VSS	TEST4	AF
	14	15	16	17	18	19	20	21	22	23	24	25	26	



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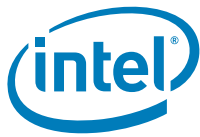


**Table 16. Pin Listing by Pin Name**  
(Sheet 1 of 16)

Pin Name	Pin Number	Signal Buffer Type	Direction
A[3]#	J4	Source Synch	Input/Output
A[4]#	L5	Source Synch	Input/Output
A[5]#	L4	Source Synch	Input/Output
A[6]#	K5	Source Synch	Input/Output
A[7]#	M3	Source Synch	Input/Output
A[8]#	N2	Source Synch	Input/Output
A[9]#	J1	Source Synch	Input/Output
A[10]#	N3	Source Synch	Input/Output
A[11]#	P5	Source Synch	Input/Output
A[12]#	P2	Source Synch	Input/Output
A[13]#	L2	Source Synch	Input/Output
A[14]#	P4	Source Synch	Input/Output
A[15]#	P1	Source Synch	Input/Output
A[16]#	R1	Source Synch	Input/Output
A[17]#	Y2	Source Synch	Input/Output
A[18]#	U5	Source Synch	Input/Output
A[19]#	R3	Source Synch	Input/Output
A[20]#	W6	Source Synch	Input/Output
A[21]#	U4	Source Synch	Input/Output
A[22]#	Y5	Source Synch	Input/Output
A[23]#	U1	Source Synch	Input/Output

**Table 16. Pin Listing by Pin Name**  
(Sheet 2 of 16)

Pin Name	Pin Number	Signal Buffer Type	Direction
A[24]#	R4	Source Synch	Input/Output
A[25]#	T5	Source Synch	Input/Output
A[26]#	T3	Source Synch	Input/Output
A[27]#	W2	Source Synch	Input/Output
A[28]#	W5	Source Synch	Input/Output
A[29]#	Y4	Source Synch	Input/Output
A[30]#	U2	Source Synch	Input/Output
A[31]#	V4	Source Synch	Input/Output
A[32]#	W3	Source Synch	Input/Output
A[33]#	AA4	Source Synch	Input/Output
A[34]#	AB2	Source Synch	Input/Output
A[35]#	AA3	Source Synch	Input/Output
A20M#	A6	CMOS	Input
ADS#	H1	Common Clock	Input/Output
ADSTB[0]#	M1	Source Synch	Input/Output
ADSTB[1]#	V1	Source Synch	Input/Output
BCLK[0]	A22	Bus Clock	Input
BCLK[1]	A21	Bus Clock	Input
BNR#	E2	Common Clock	Input/Output
BPM[0]#	AD4	Common Clock	Input/Output
BPM[1]#	AD3	Common Clock	Output
BPM[2]#	AD1	Common Clock	Output
BPM[3]#	AC4	Common Clock	Input/Output
BPRI#	G5	Common Clock	Input



**Table 16. Pin Listing by Pin Name  
(Sheet 3 of 16)**

Pin Name	Pin Number	Signal Buffer Type	Direction
BR0#	F1	Common Clock	Input/ Output
BSEL[0]	B22	CMOS	Output
BSEL[1]	B23	CMOS	Output
BSEL[2]	C21	CMOS	Output
COMP[0]	R26	Power/Other	Input/ Output
COMP[1]	U26	Power/Other	Input/ Output
COMP[2]	AA1	Power/Other	Input/ Output
COMP[3]	Y1	Power/Other	Input/ Output
D[0]#	E22	Source Synch	Input/ Output
D[1]#	F24	Source Synch	Input/ Output
D[2]#	E26	Source Synch	Input/ Output
D[3]#	G22	Source Synch	Input/ Output
D[4]#	F23	Source Synch	Input/ Output
D[5]#	G25	Source Synch	Input/ Output
D[6]#	E25	Source Synch	Input/ Output
D[7]#	E23	Source Synch	Input/ Output
D[8]#	K24	Source Synch	Input/ Output
D[9]#	G24	Source Synch	Input/ Output
D[10]#	J24	Source Synch	Input/ Output
D[11]#	J23	Source Synch	Input/ Output
D[12]#	H22	Source Synch	Input/ Output
D[13]#	F26	Source Synch	Input/ Output
D[14]#	K22	Source Synch	Input/ Output

**Table 16. Pin Listing by Pin Name  
(Sheet 4 of 16)**

Pin Name	Pin Number	Signal Buffer Type	Direction
D[15]#	H23	Source Synch	Input/ Output
D[16]#	N22	Source Synch	Input/ Output
D[17]#	K25	Source Synch	Input/ Output
D[18]#	P26	Source Synch	Input/ Output
D[19]#	R23	Source Synch	Input/ Output
D[20]#	L23	Source Synch	Input/ Output
D[21]#	M24	Source Synch	Input/ Output
D[22]#	L22	Source Synch	Input/ Output
D[23]#	M23	Source Synch	Input/ Output
D[24]#	P25	Source Synch	Input/ Output
D[25]#	P23	Source Synch	Input/ Output
D[26]#	P22	Source Synch	Input/ Output
D[27]#	T24	Source Synch	Input/ Output
D[28]#	R24	Source Synch	Input/ Output
D[29]#	L25	Source Synch	Input/ Output
D[30]#	T25	Source Synch	Input/ Output
D[31]#	N25	Source Synch	Input/ Output
D[32]#	Y22	Source Synch	Input/ Output
D[33]#	AB24	Source Synch	Input/ Output
D[34]#	V24	Source Synch	Input/ Output
D[35]#	V26	Source Synch	Input/ Output
D[36]#	V23	Source Synch	Input/ Output


**Table 16. Pin Listing by Pin Name**  
 (Sheet 5 of 16)

Pin Name	Pin Number	Signal Buffer Type	Direction
D[37]#	T22	Source Synch	Input/Output
D[38]#	U25	Source Synch	Input/Output
D[39]#	U23	Source Synch	Input/Output
D[40]#	Y25	Source Synch	Input/Output
D[41]#	W22	Source Synch	Input/Output
D[42]#	Y23	Source Synch	Input/Output
D[43]#	W24	Source Synch	Input/Output
D[44]#	W25	Source Synch	Input/Output
D[45]#	AA23	Source Synch	Input/Output
D[46]#	AA24	Source Synch	Input/Output
D[47]#	AB25	Source Synch	Input/Output
D[48]#	AE24	Source Synch	Input/Output
D[49]#	AD24	Source Synch	Input/Output
D[50]#	AA21	Source Synch	Input/Output
D[51]#	AB22	Source Synch	Input/Output
D[52]#	AB21	Source Synch	Input/Output
D[53]#	AC26	Source Synch	Input/Output
D[54]#	AD20	Source Synch	Input/Output
D[55]#	AE22	Source Synch	Input/Output
D[56]#	AF23	Source Synch	Input/Output
D[57]#	AC25	Source Synch	Input/Output
D[58]#	AE21	Source Synch	Input/Output

**Table 16. Pin Listing by Pin Name**  
 (Sheet 6 of 16)

Pin Name	Pin Number	Signal Buffer Type	Direction
D[59]#	AD21	Source Synch	Input/Output
D[60]#	AC22	Source Synch	Input/Output
D[61]#	AD23	Source Synch	Input/Output
D[62]#	AF22	Source Synch	Input/Output
D[63]#	AC23	Source Synch	Input/Output
DBR#	C20	CMOS	Output
DBSY#	E1	Common Clock	Input/Output
DEFER#	H5	Common Clock	Input
DINV[0]#	H25	Source Synch	Input/Output
DINV[1]#	N24	Source Synch	Input/Output
DINV[2]#	U22	Source Synch	Input/Output
DINV[3]#	AC20	Source Synch	Input/Output
DPRSTP#	E5	CMOS	Input
DPSLP#	B5	CMOS	Input
DPWR#	D24	Common Clock	Input/Output
DRDY#	F21	Common Clock	Input/Output
DSTBN[0]#	J26	Source Synch	Input/Output
DSTBN[1]#	L26	Source Synch	Input/Output
DSTBN[2]#	Y26	Source Synch	Input/Output
DSTBN[3]#	AE25	Source Synch	Input/Output
DSTBP[0]#	H26	Source Synch	Input/Output
DSTBP[1]#	M26	Source Synch	Input/Output
DSTBP[2]#	AA26	Source Synch	Input/Output



**Table 16. Pin Listing by Pin Name  
(Sheet 7 of 16)**

Pin Name	Pin Number	Signal Buffer Type	Direction
DSTBP[3]#	AF24	Source Synch	Input/Output
FERR#	A5	Open Drain	Output
GTLREF	AD26	Power/Other	Input
HIT#	G6	Common Clock	Input/Output
HITM#	E4	Common Clock	Input/Output
IERR#	D20	Open Drain	Output
IGNNE#	C4	CMOS	Input
INIT#	B3	CMOS	Input
LINT0	C6	CMOS	Input
LINT1	B4	CMOS	Input
LOCK#	H4	Common Clock	Input/Output
PRDY#	AC2	Common Clock	Output
PREQ#	AC1	Common Clock	Input
PROCHOT#	D21	Open Drain	Input/Output
PSI#	AE6	CMOS	Output
PWRGOOD	D6	CMOS	Input
REQ[0]#	K3	Source Synch	Input/Output
REQ[1]#	H2	Source Synch	Input/Output
REQ[2]#	K2	Source Synch	Input/Output
REQ[3]#	J3	Source Synch	Input/Output
REQ[4]#	L1	Source Synch	Input/Output
RESET#	C1	Common Clock	Input
RS[0]#	F3	Common Clock	Input
RS[1]#	F4	Common Clock	Input
RS[2]#	G3	Common Clock	Input
RSVD	B2	Reserved	
RSVD	C3	Reserved	
RSVD	D2	Reserved	
RSVD	D3	Reserved	
RSVD	D22	Reserved	

**Table 16. Pin Listing by Pin Name  
(Sheet 8 of 16)**

Pin Name	Pin Number	Signal Buffer Type	Direction
RSVD	F6	Reserved	
RSVD	M4	Reserved	
RSVD	N5	Reserved	
RSVD	T2	Reserved	
RSVD	V3	Reserved	
SLP#	D7	CMOS	Input
SMI#	A3	CMOS	Input
STPCLK#	D5	CMOS	Input
TCK	AC5	CMOS	Input
TDI	AA6	CMOS	Input
TDO	AB3	Open Drain	Output
TEST1	C23	Test	
TEST2	D25	Test	
TEST3	C24	Test	
TEST4	AF26	Test	
TEST5	AF1	Test	
TEST6	A26	Test	
THERMTRIP#	C7	Open Drain	Output
THRMDA	A24	Power/Other	
THRMDC	B25	Power/Other	
TMS	AB5	CMOS	Input
TRDY#	G2	Common Clock	Input
TRST#	AB6	CMOS	Input
VCC	A7	Power/Other	
VCC	A9	Power/Other	
VCC	A10	Power/Other	
VCC	A12	Power/Other	
VCC	A13	Power/Other	
VCC	A15	Power/Other	
VCC	A17	Power/Other	
VCC	A18	Power/Other	
VCC	A20	Power/Other	
VCC	AA7	Power/Other	
VCC	AA9	Power/Other	
VCC	AA10	Power/Other	
VCC	AA12	Power/Other	




**Table 16. Pin Listing by Pin Name**  
 (Sheet 9 of 16)

Pin Name	Pin Number	Signal Buffer Type	Direction
VCC	AA13	Power/Other	
VCC	AA15	Power/Other	
VCC	AA17	Power/Other	
VCC	AA18	Power/Other	
VCC	AA20	Power/Other	
VCC	AB7	Power/Other	
VCC	AB9	Power/Other	
VCC	AB10	Power/Other	
VCC	AB12	Power/Other	
VCC	AB14	Power/Other	
VCC	AB15	Power/Other	
VCC	AB17	Power/Other	
VCC	AB18	Power/Other	
VCC	AB20	Power/Other	
VCC	AC7	Power/Other	
VCC	AC9	Power/Other	
VCC	AC10	Power/Other	
VCC	AC12	Power/Other	
VCC	AC13	Power/Other	
VCC	AC15	Power/Other	
VCC	AC17	Power/Other	
VCC	AC18	Power/Other	
VCC	AD7	Power/Other	
VCC	AD9	Power/Other	
VCC	AD10	Power/Other	
VCC	AD12	Power/Other	
VCC	AD14	Power/Other	
VCC	AD15	Power/Other	
VCC	AD17	Power/Other	
VCC	AD18	Power/Other	
VCC	AE9	Power/Other	
VCC	AE10	Power/Other	
VCC	AE12	Power/Other	
VCC	AE13	Power/Other	
VCC	AE15	Power/Other	
VCC	AE17	Power/Other	

**Table 16. Pin Listing by Pin Name**  
 (Sheet 10 of 16)

Pin Name	Pin Number	Signal Buffer Type	Direction
VCC	AE18	Power/Other	
VCC	AE20	Power/Other	
VCC	AF9	Power/Other	
VCC	AF10	Power/Other	
VCC	AF12	Power/Other	
VCC	AF14	Power/Other	
VCC	AF15	Power/Other	
VCC	AF17	Power/Other	
VCC	AF18	Power/Other	
VCC	AF20	Power/Other	
VCC	B7	Power/Other	
VCC	B9	Power/Other	
VCC	B10	Power/Other	
VCC	B12	Power/Other	
VCC	B14	Power/Other	
VCC	B15	Power/Other	
VCC	B17	Power/Other	
VCC	B18	Power/Other	
VCC	B20	Power/Other	
VCC	C9	Power/Other	
VCC	C10	Power/Other	
VCC	C12	Power/Other	
VCC	C13	Power/Other	
VCC	C15	Power/Other	
VCC	C17	Power/Other	
VCC	C18	Power/Other	
VCC	D9	Power/Other	
VCC	D10	Power/Other	
VCC	D12	Power/Other	
VCC	D14	Power/Other	
VCC	D15	Power/Other	
VCC	D17	Power/Other	
VCC	D18	Power/Other	
VCC	E7	Power/Other	
VCC	E9	Power/Other	
VCC	E10	Power/Other	



**Table 16. Pin Listing by Pin Name  
(Sheet 11 of 16)**

Pin Name	Pin Number	Signal Buffer Type	Direction
VCC	E12	Power/Other	
VCC	E13	Power/Other	
VCC	E15	Power/Other	
VCC	E17	Power/Other	
VCC	E18	Power/Other	
VCC	E20	Power/Other	
VCC	F7	Power/Other	
VCC	F9	Power/Other	
VCC	F10	Power/Other	
VCC	F12	Power/Other	
VCC	F14	Power/Other	
VCC	F15	Power/Other	
VCC	F17	Power/Other	
VCC	F18	Power/Other	
VCC	F20	Power/Other	
VCCA	B26	Power/Other	
VCCA	C26	Power/Other	
VCCP	G21	Power/Other	
VCCP	J6	Power/Other	
VCCP	J21	Power/Other	
VCCP	K6	Power/Other	
VCCP	K21	Power/Other	
VCCP	M6	Power/Other	
VCCP	M21	Power/Other	
VCCP	N6	Power/Other	
VCCP	N21	Power/Other	
VCCP	R6	Power/Other	
VCCP	R21	Power/Other	
VCCP	T6	Power/Other	
VCCP	T21	Power/Other	
VCCP	V6	Power/Other	
VCCP	V21	Power/Other	
VCCP	W21	Power/Other	
VCCSENSE	AF7	Power/Other	
VID[0]	AD6	CMOS	Output
VID[1]	AF5	CMOS	Output

**Table 16. Pin Listing by Pin Name  
(Sheet 12 of 16)**

Pin Name	Pin Number	Signal Buffer Type	Direction
VID[2]	AE5	CMOS	Output
VID[3]	AF4	CMOS	Output
VID[4]	AE3	CMOS	Output
VID[5]	AF3	CMOS	Output
VID[6]	AE2	CMOS	Output
VSS	A2	Power/Other	
VSS	A4	Power/Other	
VSS	A8	Power/Other	
VSS	A11	Power/Other	
VSS	A14	Power/Other	
VSS	A16	Power/Other	
VSS	A19	Power/Other	
VSS	A23	Power/Other	
VSS	A25	Power/Other	
VSS	AA2	Power/Other	
VSS	AA5	Power/Other	
VSS	AA8	Power/Other	
VSS	AA11	Power/Other	
VSS	AA14	Power/Other	
VSS	AA16	Power/Other	
VSS	AA19	Power/Other	
VSS	AA22	Power/Other	
VSS	AA25	Power/Other	
VSS	AB1	Power/Other	
VSS	AB4	Power/Other	
VSS	AB8	Power/Other	
VSS	AB11	Power/Other	
VSS	AB13	Power/Other	
VSS	AB16	Power/Other	
VSS	AB19	Power/Other	
VSS	AB23	Power/Other	
VSS	AB26	Power/Other	
VSS	AC3	Power/Other	
VSS	AC6	Power/Other	
VSS	AC8	Power/Other	
VSS	AC11	Power/Other	


**Table 16. Pin Listing by Pin Name**  
**(Sheet 13 of 16)**

Pin Name	Pin Number	Signal Buffer Type	Direction
VSS	AC14	Power/Other	
VSS	AC16	Power/Other	
VSS	AC19	Power/Other	
VSS	AC21	Power/Other	
VSS	AC24	Power/Other	
VSS	AD2	Power/Other	
VSS	AD5	Power/Other	
VSS	AD8	Power/Other	
VSS	AD11	Power/Other	
VSS	AD13	Power/Other	
VSS	AD16	Power/Other	
VSS	AD19	Power/Other	
VSS	AD22	Power/Other	
VSS	AD25	Power/Other	
VSS	AE1	Power/Other	
VSS	AE4	Power/Other	
VSS	AE8	Power/Other	
VSS	AE11	Power/Other	
VSS	AE14	Power/Other	
VSS	AE16	Power/Other	
VSS	AE19	Power/Other	
VSS	AE23	Power/Other	
VSS	AE26	Power/Other	
VSS	AF2	Power/Other	
VSS	AF6	Power/Other	
VSS	AF8	Power/Other	
VSS	AF11	Power/Other	
VSS	AF13	Power/Other	
VSS	AF16	Power/Other	
VSS	AF19	Power/Other	
VSS	AF21	Power/Other	
VSS	AF25	Power/Other	
VSS	B6	Power/Other	
VSS	B8	Power/Other	
VSS	B11	Power/Other	
VSS	B13	Power/Other	

**Table 16. Pin Listing by Pin Name**  
**(Sheet 14 of 16)**

Pin Name	Pin Number	Signal Buffer Type	Direction
VSS	B16	Power/Other	
VSS	B19	Power/Other	
VSS	B21	Power/Other	
VSS	B24	Power/Other	
VSS	C2	Power/Other	
VSS	C5	Power/Other	
VSS	C8	Power/Other	
VSS	C11	Power/Other	
VSS	C14	Power/Other	
VSS	C16	Power/Other	
VSS	C19	Power/Other	
VSS	C22	Power/Other	
VSS	C25	Power/Other	
VSS	D1	Power/Other	
VSS	D4	Power/Other	
VSS	D8	Power/Other	
VSS	D11	Power/Other	
VSS	D13	Power/Other	
VSS	D16	Power/Other	
VSS	D19	Power/Other	
VSS	D23	Power/Other	
VSS	D26	Power/Other	
VSS	E3	Power/Other	
VSS	E6	Power/Other	
VSS	E8	Power/Other	
VSS	E11	Power/Other	
VSS	E14	Power/Other	
VSS	E16	Power/Other	
VSS	E19	Power/Other	
VSS	E21	Power/Other	
VSS	E24	Power/Other	
VSS	F2	Power/Other	
VSS	F5	Power/Other	
VSS	F8	Power/Other	
VSS	F11	Power/Other	
VSS	F13	Power/Other	



**Table 16. Pin Listing by Pin Name  
(Sheet 15 of 16)**

Pin Name	Pin Number	Signal Buffer Type	Direction
VSS	F16	Power/Other	
VSS	F19	Power/Other	
VSS	F22	Power/Other	
VSS	F25	Power/Other	
VSS	G1	Power/Other	
VSS	G4	Power/Other	
VSS	G23	Power/Other	
VSS	G26	Power/Other	
VSS	H3	Power/Other	
VSS	H6	Power/Other	
VSS	H21	Power/Other	
VSS	H24	Power/Other	
VSS	J2	Power/Other	
VSS	J5	Power/Other	
VSS	J22	Power/Other	
VSS	J25	Power/Other	
VSS	K1	Power/Other	
VSS	K4	Power/Other	
VSS	K23	Power/Other	
VSS	K26	Power/Other	
VSS	L3	Power/Other	
VSS	L6	Power/Other	
VSS	L21	Power/Other	
VSS	L24	Power/Other	
VSS	M2	Power/Other	
VSS	M5	Power/Other	
VSS	M22	Power/Other	
VSS	M25	Power/Other	
VSS	N1	Power/Other	
VSS	N4	Power/Other	
VSS	N23	Power/Other	
VSS	N26	Power/Other	
VSS	P3	Power/Other	
VSS	P6	Power/Other	
VSS	P21	Power/Other	
VSS	P24	Power/Other	

**Table 16. Pin Listing by Pin Name  
(Sheet 16 of 16)**

Pin Name	Pin Number	Signal Buffer Type	Direction
VSS	R2	Power/Other	
VSS	R5	Power/Other	
VSS	R22	Power/Other	
VSS	R25	Power/Other	
VSS	T1	Power/Other	
VSS	T4	Power/Other	
VSS	T23	Power/Other	
VSS	T26	Power/Other	
VSS	U3	Power/Other	
VSS	U6	Power/Other	
VSS	U21	Power/Other	
VSS	U24	Power/Other	
VSS	V2	Power/Other	
VSS	V5	Power/Other	
VSS	V22	Power/Other	
VSS	V25	Power/Other	
VSS	W1	Power/Other	
VSS	W4	Power/Other	
VSS	W23	Power/Other	
VSS	W26	Power/Other	
VSS	Y3	Power/Other	
VSS	Y6	Power/Other	
VSS	Y21	Power/Other	
VSS	Y24	Power/Other	
VSSSENSE	AE7	Power/Other	Output

**Table 17. Pin Listing by Pin Number  
(Sheet 1 of 17)**

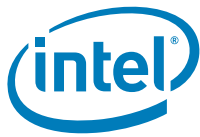
Pin Name	Pin Number	Signal Buffer Type	Direction
VSS	A2	Power/Other	
SMI#	A3	CMOS	Input
VSS	A4	Power/Other	
FERR#	A5	Open Drain	Output
A20M#	A6	CMOS	Input
VCC	A7	Power/Other	


**Table 17. Pin Listing by Pin Number**  
**(Sheet 2 of 17)**

Pin Name	Pin Number	Signal Buffer Type	Direction
VSS	A8	Power/Other	
VCC	A9	Power/Other	
VCC	A10	Power/Other	
VSS	A11	Power/Other	
VCC	A12	Power/Other	
VCC	A13	Power/Other	
VSS	A14	Power/Other	
VCC	A15	Power/Other	
VSS	A16	Power/Other	
VCC	A17	Power/Other	
VCC	A18	Power/Other	
VSS	A19	Power/Other	
VCC	A20	Power/Other	
BCLK[1]	A21	Bus Clock	Input
BCLK[0]	A22	Bus Clock	Input
VSS	A23	Power/Other	
THRMDA	A24	Power/Other	
VSS	A25	Power/Other	
TEST6	A26	Test	
COMP[2]	AA1	Power/Other	Input/Output
VSS	AA2	Power/Other	
A[35]#	AA3	Source Synch	Input/Output
A[33]#	AA4	Source Synch	Input/Output
VSS	AA5	Power/Other	
TDI	AA6	CMOS	Input
VCC	AA7	Power/Other	
VSS	AA8	Power/Other	
VCC	AA9	Power/Other	
VCC	AA10	Power/Other	
VSS	AA11	Power/Other	
VCC	AA12	Power/Other	
VCC	AA13	Power/Other	
VSS	AA14	Power/Other	
VCC	AA15	Power/Other	

**Table 17. Pin Listing by Pin Number**  
**(Sheet 3 of 17)**

Pin Name	Pin Number	Signal Buffer Type	Direction
VSS	AA16	Power/Other	
VCC	AA17	Power/Other	
VCC	AA18	Power/Other	
VSS	AA19	Power/Other	
VCC	AA20	Power/Other	
D[50]#	AA21	Source Synch	Input/Output
VSS	AA22	Power/Other	
D[45]#	AA23	Source Synch	Input/Output
D[46]#	AA24	Source Synch	Input/Output
VSS	AA25	Power/Other	
DSTBP[2]#	AA26	Source Synch	Input/Output
VSS	AB1	Power/Other	
A[34]#	AB2	Source Synch	Input/Output
TDO	AB3	Open Drain	Output
VSS	AB4	Power/Other	
TMS	AB5	CMOS	Input
TRST#	AB6	CMOS	Input
VCC	AB7	Power/Other	
VSS	AB8	Power/Other	
VCC	AB9	Power/Other	
VCC	AB10	Power/Other	
VSS	AB11	Power/Other	
VCC	AB12	Power/Other	
VSS	AB13	Power/Other	
VCC	AB14	Power/Other	
VCC	AB15	Power/Other	
VSS	AB16	Power/Other	
VCC	AB17	Power/Other	
VCC	AB18	Power/Other	
VSS	AB19	Power/Other	
VCC	AB20	Power/Other	
D[52]#	AB21	Source Synch	Input/Output



**Table 17. Pin Listing by Pin Number  
(Sheet 4 of 17)**

Pin Name	Pin Number	Signal Buffer Type	Direction
D[51]#	AB22	Source Synch	Input/Output
VSS	AB23	Power/Other	
D[33]#	AB24	Source Synch	Input/Output
D[47]#	AB25	Source Synch	Input/Output
VSS	AB26	Power/Other	
PREQ#	AC1	Common Clock	Input
PRDY#	AC2	Common Clock	Output
VSS	AC3	Power/Other	
BPM[3]#	AC4	Common Clock	Input/Output
TCK	AC5	CMOS	Input
VSS	AC6	Power/Other	
VCC	AC7	Power/Other	
VSS	AC8	Power/Other	
VCC	AC9	Power/Other	
VCC	AC10	Power/Other	
VSS	AC11	Power/Other	
VCC	AC12	Power/Other	
VCC	AC13	Power/Other	
VSS	AC14	Power/Other	
VCC	AC15	Power/Other	
VSS	AC16	Power/Other	
VCC	AC17	Power/Other	
VCC	AC18	Power/Other	
VSS	AC19	Power/Other	
DINV[3]#	AC20	Source Synch	Input/Output
VSS	AC21	Power/Other	
D[60]#	AC22	Source Synch	Input/Output
D[63]#	AC23	Source Synch	Input/Output
VSS	AC24	Power/Other	
D[57]#	AC25	Source Synch	Input/Output

**Table 17. Pin Listing by Pin Number  
(Sheet 5 of 17)**

Pin Name	Pin Number	Signal Buffer Type	Direction
D[53]#	AC26	Source Synch	Input/Output
BPM[2]#	AD1	Common Clock	Output
VSS	AD2	Power/Other	
BPM[1]#	AD3	Common Clock	Output
BPM[0]#	AD4	Common Clock	Input/Output
VSS	AD5	Power/Other	
VID[0]	AD6	CMOS	Output
VCC	AD7	Power/Other	
VSS	AD8	Power/Other	
VCC	AD9	Power/Other	
VCC	AD10	Power/Other	
VSS	AD11	Power/Other	
VCC	AD12	Power/Other	
VSS	AD13	Power/Other	
VCC	AD14	Power/Other	
VCC	AD15	Power/Other	
VSS	AD16	Power/Other	
VCC	AD17	Power/Other	
VCC	AD18	Power/Other	
VSS	AD19	Power/Other	
D[54]#	AD20	Source Synch	Input/Output
D[59]#	AD21	Source Synch	Input/Output
VSS	AD22	Power/Other	
D[61]#	AD23	Source Synch	Input/Output
D[49]#	AD24	Source Synch	Input/Output
VSS	AD25	Power/Other	
GTLREF	AD26	Power/Other	Input
VSS	AE1	Power/Other	
VID[6]	AE2	CMOS	Output
VID[4]	AE3	CMOS	Output
VSS	AE4	Power/Other	


**Table 17. Pin Listing by Pin Number**  
 (Sheet 6 of 17)

Pin Name	Pin Number	Signal Buffer Type	Direction
VID[2]	AE5	CMOS	Output
PSI#	AE6	CMOS	Output
VSSSENSE	AE7	Power/Other	Output
VSS	AE8	Power/Other	
VCC	AE9	Power/Other	
VCC	AE10	Power/Other	
VSS	AE11	Power/Other	
VCC	AE12	Power/Other	
VCC	AE13	Power/Other	
VSS	AE14	Power/Other	
VCC	AE15	Power/Other	
VSS	AE16	Power/Other	
VCC	AE17	Power/Other	
VCC	AE18	Power/Other	
VSS	AE19	Power/Other	
VCC	AE20	Power/Other	
D[58]#	AE21	Source Synch	Input/Output
D[55]#	AE22	Source Synch	Input/Output
VSS	AE23	Power/Other	
D[48]#	AE24	Source Synch	Input/Output
DSTBN[3]#	AE25	Source Synch	Input/Output
VSS	AE26	Power/Other	
TEST5	AF1	Test	
VSS	AF2	Power/Other	
VID[5]	AF3	CMOS	Output
VID[3]	AF4	CMOS	Output
VID[1]	AF5	CMOS	Output
VSS	AF6	Power/Other	
VCCSENSE	AF7	Power/Other	
VSS	AF8	Power/Other	
VCC	AF9	Power/Other	
VCC	AF10	Power/Other	
VSS	AF11	Power/Other	
VCC	AF12	Power/Other	

**Table 17. Pin Listing by Pin Number**  
 (Sheet 7 of 17)

Pin Name	Pin Number	Signal Buffer Type	Direction
VSS	AF13	Power/Other	
VCC	AF14	Power/Other	
VCC	AF15	Power/Other	
VSS	AF16	Power/Other	
VCC	AF17	Power/Other	
VCC	AF18	Power/Other	
VSS	AF19	Power/Other	
VCC	AF20	Power/Other	
VSS	AF21	Power/Other	
D[62]#	AF22	Source Synch	Input/Output
D[56]#	AF23	Source Synch	Input/Output
DSTBP[3]#	AF24	Source Synch	Input/Output
VSS	AF25	Power/Other	
TEST4	AF26	Test	
RSVD	B2	Reserved	
INIT#	B3	CMOS	Input
LINT1	B4	CMOS	Input
DPSLP#	B5	CMOS	Input
VSS	B6	Power/Other	
VCC	B7	Power/Other	
VSS	B8	Power/Other	
VCC	B9	Power/Other	
VCC	B10	Power/Other	
VSS	B11	Power/Other	
VCC	B12	Power/Other	
VSS	B13	Power/Other	
VCC	B14	Power/Other	
VCC	B15	Power/Other	
VSS	B16	Power/Other	
VCC	B17	Power/Other	
VCC	B18	Power/Other	
VSS	B19	Power/Other	
VCC	B20	Power/Other	
VSS	B21	Power/Other	



**Table 17. Pin Listing by Pin Number  
(Sheet 8 of 17)**

Pin Name	Pin Number	Signal Buffer Type	Direction
BSEL[0]	B22	CMOS	Output
BSEL[1]	B23	CMOS	Output
VSS	B24	Power/Other	
THRMDC	B25	Power/Other	
VCCA	B26	Power/Other	
RESET#	C1	Common Clock	Input
VSS	C2	Power/Other	
RSVD	C3	Reserved	
IGNNE#	C4	CMOS	Input
VSS	C5	Power/Other	
LINT0	C6	CMOS	Input
THERMTRIP #	C7	Open Drain	Output
VSS	C8	Power/Other	
VCC	C9	Power/Other	
VCC	C10	Power/Other	
VSS	C11	Power/Other	
VCC	C12	Power/Other	
VCC	C13	Power/Other	
VSS	C14	Power/Other	
VCC	C15	Power/Other	
VSS	C16	Power/Other	
VCC	C17	Power/Other	
VCC	C18	Power/Other	
VSS	C19	Power/Other	
DBR#	C20	CMOS	Output
BSEL[2]	C21	CMOS	Output
VSS	C22	Power/Other	
TEST1	C23	Test	
TEST3	C24	Test	
VSS	C25	Power/Other	
VCCA	C26	Power/Other	
VSS	D1	Power/Other	
RSVD	D2	Reserved	
RSVD	D3	Reserved	
VSS	D4	Power/Other	

**Table 17. Pin Listing by Pin Number  
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Pin Name	Pin Number	Signal Buffer Type	Direction
STPCLK#	D5	CMOS	Input
PWRGOOD	D6	CMOS	Input
SLP#	D7	CMOS	Input
VSS	D8	Power/Other	
VCC	D9	Power/Other	
VCC	D10	Power/Other	
VSS	D11	Power/Other	
VCC	D12	Power/Other	
VSS	D13	Power/Other	
VCC	D14	Power/Other	
VCC	D15	Power/Other	
VSS	D16	Power/Other	
VCC	D17	Power/Other	
VCC	D18	Power/Other	
VSS	D19	Power/Other	
IERR#	D20	Open Drain	Output
PROCHOT#	D21	Open Drain	Input/Output
RSVD	D22	Reserved	
VSS	D23	Power/Other	
DPWR#	D24	Common Clock	Input/Output
TEST2	D25	Test	
VSS	D26	Power/Other	
DBSY#	E1	Common Clock	Input/Output
BNR#	E2	Common Clock	Input/Output
VSS	E3	Power/Other	
HITM#	E4	Common Clock	Input/Output
DPRSTP#	E5	CMOS	Input
VSS	E6	Power/Other	
VCC	E7	Power/Other	
VSS	E8	Power/Other	
VCC	E9	Power/Other	
VCC	E10	Power/Other	
VSS	E11	Power/Other	




**Table 17. Pin Listing by Pin Number**  
**(Sheet 10 of 17)**

Pin Name	Pin Number	Signal Buffer Type	Direction
VCC	E12	Power/Other	
VCC	E13	Power/Other	
VSS	E14	Power/Other	
VCC	E15	Power/Other	
VSS	E16	Power/Other	
VCC	E17	Power/Other	
VCC	E18	Power/Other	
VSS	E19	Power/Other	
VCC	E20	Power/Other	
VSS	E21	Power/Other	
D[0]#	E22	Source Synch	Input/Output
D[7]#	E23	Source Synch	Input/Output
VSS	E24	Power/Other	
D[6]#	E25	Source Synch	Input/Output
D[2]#	E26	Source Synch	Input/Output
BR0#	F1	Common Clock	Input/Output
VSS	F2	Power/Other	
RS[0]#	F3	Common Clock	Input
RS[1]#	F4	Common Clock	Input
VSS	F5	Power/Other	
RSVD	F6	Reserved	
VCC	F7	Power/Other	
VSS	F8	Power/Other	
VCC	F9	Power/Other	
VCC	F10	Power/Other	
VSS	F11	Power/Other	
VCC	F12	Power/Other	
VSS	F13	Power/Other	
VCC	F14	Power/Other	
VCC	F15	Power/Other	
VSS	F16	Power/Other	
VCC	F17	Power/Other	

**Table 17. Pin Listing by Pin Number**  
**(Sheet 11 of 17)**

Pin Name	Pin Number	Signal Buffer Type	Direction
VCC	F18	Power/Other	
VSS	F19	Power/Other	
VCC	F20	Power/Other	
DRDY#	F21	Common Clock	Input/Output
VSS	F22	Power/Other	
D[4]#	F23	Source Synch	Input/Output
D[1]#	F24	Source Synch	Input/Output
VSS	F25	Power/Other	
D[13]#	F26	Source Synch	Input/Output
VSS	G1	Power/Other	
TRDY#	G2	Common Clock	Input
RS[2]#	G3	Common Clock	Input
VSS	G4	Power/Other	
BPRI#	G5	Common Clock	Input
HIT#	G6	Common Clock	Input/Output
VCCP	G21	Power/Other	
D[3]#	G22	Source Synch	Input/Output
VSS	G23	Power/Other	
D[9]#	G24	Source Synch	Input/Output
D[5]#	G25	Source Synch	Input/Output
VSS	G26	Power/Other	
ADS#	H1	Common Clock	Input/Output
REQ[1]#	H2	Source Synch	Input/Output
VSS	H3	Power/Other	
LOCK#	H4	Common Clock	Input/Output
DEFER#	H5	Common Clock	Input



**Table 17. Pin Listing by Pin Number  
(Sheet 12 of 17)**

Pin Name	Pin Number	Signal Buffer Type	Direction
VSS	H6	Power/Other	
VSS	H21	Power/Other	
D[12]#	H22	Source Synch	Input/Output
D[15]#	H23	Source Synch	Input/Output
VSS	H24	Power/Other	
DINV[0]#	H25	Source Synch	Input/Output
DSTBP[0]#	H26	Source Synch	Input/Output
A[9]#	J1	Source Synch	Input/Output
VSS	J2	Power/Other	
REQ[3]#	J3	Source Synch	Input/Output
A[3]#	J4	Source Synch	Input/Output
VSS	J5	Power/Other	
VCCP	J6	Power/Other	
VCCP	J21	Power/Other	
VSS	J22	Power/Other	
D[11]#	J23	Source Synch	Input/Output
D[10]#	J24	Source Synch	Input/Output
VSS	J25	Power/Other	
DSTBN[0]#	J26	Source Synch	Input/Output
VSS	K1	Power/Other	
REQ[2]#	K2	Source Synch	Input/Output
REQ[0]#	K3	Source Synch	Input/Output
VSS	K4	Power/Other	
A[6]#	K5	Source Synch	Input/Output
VCCP	K6	Power/Other	
VCCP	K21	Power/Other	
D[14]#	K22	Source Synch	Input/Output

**Table 17. Pin Listing by Pin Number  
(Sheet 13 of 17)**

Pin Name	Pin Number	Signal Buffer Type	Direction
VSS	K23	Power/Other	
D[8]#	K24	Source Synch	Input/Output
D[17]#	K25	Source Synch	Input/Output
VSS	K26	Power/Other	
REQ[4]#	L1	Source Synch	Input/Output
A[13]#	L2	Source Synch	Input/Output
VSS	L3	Power/Other	
A[5]#	L4	Source Synch	Input/Output
A[4]#	L5	Source Synch	Input/Output
VSS	L6	Power/Other	
VSS	L21	Power/Other	
D[22]#	L22	Source Synch	Input/Output
D[20]#	L23	Source Synch	Input/Output
VSS	L24	Power/Other	
D[29]#	L25	Source Synch	Input/Output
DSTBN[1]#	L26	Source Synch	Input/Output
ADSTB[0]#	M1	Source Synch	Input/Output
VSS	M2	Power/Other	
A[7]#	M3	Source Synch	Input/Output
RSVD	M4	Reserved	
VSS	M5	Power/Other	
VCCP	M6	Power/Other	
VCCP	M21	Power/Other	
VSS	M22	Power/Other	
D[23]#	M23	Source Synch	Input/Output
D[21]#	M24	Source Synch	Input/Output
VSS	M25	Power/Other	


**Table 17. Pin Listing by Pin Number**  
 (Sheet 14 of 17)

Pin Name	Pin Number	Signal Buffer Type	Direction
DSTBP[1]#	M26	Source Synch	Input/Output
VSS	N1	Power/Other	
A[8]#	N2	Source Synch	Input/Output
A[10]#	N3	Source Synch	Input/Output
VSS	N4	Power/Other	
RSVD	N5	Reserved	
VCCP	N6	Power/Other	
VCCP	N21	Power/Other	
D[16]#	N22	Source Synch	Input/Output
VSS	N23	Power/Other	
DINV[1]#	N24	Source Synch	Input/Output
D[31]#	N25	Source Synch	Input/Output
VSS	N26	Power/Other	
A[15]#	P1	Source Synch	Input/Output
A[12]#	P2	Source Synch	Input/Output
VSS	P3	Power/Other	
A[14]#	P4	Source Synch	Input/Output
A[11]#	P5	Source Synch	Input/Output
VSS	P6	Power/Other	
VSS	P21	Power/Other	
D[26]#	P22	Source Synch	Input/Output
D[25]#	P23	Source Synch	Input/Output
VSS	P24	Power/Other	
D[24]#	P25	Source Synch	Input/Output
D[18]#	P26	Source Synch	Input/Output
A[16]#	R1	Source Synch	Input/Output

**Table 17. Pin Listing by Pin Number**  
 (Sheet 15 of 17)

Pin Name	Pin Number	Signal Buffer Type	Direction
VSS	R2	Power/Other	
A[19]#	R3	Source Synch	Input/Output
A[24]#	R4	Source Synch	Input/Output
VSS	R5	Power/Other	
VCCP	R6	Power/Other	
VCCP	R21	Power/Other	
VSS	R22	Power/Other	
D[19]#	R23	Source Synch	Input/Output
D[28]#	R24	Source Synch	Input/Output
VSS	R25	Power/Other	
COMP[0]	R26	Power/Other	Input/Output
VSS	T1	Power/Other	
RSVD	T2	Reserved	
A[26]#	T3	Source Synch	Input/Output
VSS	T4	Power/Other	
A[25]#	T5	Source Synch	Input/Output
VCCP	T6	Power/Other	
VCCP	T21	Power/Other	
D[37]#	T22	Source Synch	Input/Output
VSS	T23	Power/Other	
D[27]#	T24	Source Synch	Input/Output
D[30]#	T25	Source Synch	Input/Output
VSS	T26	Power/Other	
A[23]#	U1	Source Synch	Input/Output
A[30]#	U2	Source Synch	Input/Output
VSS	U3	Power/Other	
A[21]#	U4	Source Synch	Input/Output



**Table 17. Pin Listing by Pin Number  
(Sheet 16 of 17)**

Pin Name	Pin Number	Signal Buffer Type	Direction
A[18]#	U5	Source Synch	Input/Output
VSS	U6	Power/Other	
VSS	U21	Power/Other	
DINV[2]#	U22	Source Synch	Input/Output
D[39]#	U23	Source Synch	Input/Output
VSS	U24	Power/Other	
D[38]#	U25	Source Synch	Input/Output
COMP[1]	U26	Power/Other	Input/Output
ADSTB[1]#	V1	Source Synch	Input/Output
VSS	V2	Power/Other	
RSVD	V3	Reserved	
A[31]#	V4	Source Synch	Input/Output
VSS	V5	Power/Other	
VCCP	V6	Power/Other	
VCCP	V21	Power/Other	
VSS	V22	Power/Other	
D[36]#	V23	Source Synch	Input/Output
D[34]#	V24	Source Synch	Input/Output
VSS	V25	Power/Other	
D[35]#	V26	Source Synch	Input/Output
VSS	W1	Power/Other	
A[27]#	W2	Source Synch	Input/Output
A[32]#	W3	Source Synch	Input/Output
VSS	W4	Power/Other	
A[28]#	W5	Source Synch	Input/Output
A[20]#	W6	Source Synch	Input/Output
VCCP	W21	Power/Other	

**Table 17. Pin Listing by Pin Number  
(Sheet 17 of 17)**

Pin Name	Pin Number	Signal Buffer Type	Direction
D[41]#	W22	Source Synch	Input/Output
VSS	W23	Power/Other	
D[43]#	W24	Source Synch	Input/Output
D[44]#	W25	Source Synch	Input/Output
VSS	W26	Power/Other	
COMP[3]	Y1	Power/Other	Input/Output
A[17]#	Y2	Source Synch	Input/Output
VSS	Y3	Power/Other	
A[29]#	Y4	Source Synch	Input/Output
A[22]#	Y5	Source Synch	Input/Output
VSS	Y6	Power/Other	
VSS	Y21	Power/Other	
D[32]#	Y22	Source Synch	Input/Output
D[42]#	Y23	Source Synch	Input/Output
VSS	Y24	Power/Other	
D[40]#	Y25	Source Synch	Input/Output
DSTBN[2]#	Y26	Source Synch	Input/Output



## 4.3 Alphabetical Signals Reference

Table 18. Signal Description (Sheet 1 of 7)

Name	Type	Description						
A[35:3]#	Input/ Output	A[35:3]# (Address) define a 2 <sup>36</sup> -byte physical memory address space. In sub-phase 1 of the address phase, these pins transmit the address of a transaction. In sub-phase 2, these pins transmit transaction type information. These signals must connect the appropriate pins of both agents on the processor FSB. A[35:3]# are source synchronous signals and are latched into the receiving buffers by ADSTB[1:0]#. Address signals are used as straps which are sampled before RESET# is deasserted.						
A20M#	Input	If A20M# (Address-20 Mask) is asserted, the processor masks physical address bit 20 (A20#) before looking up a line in any internal cache and before driving a read/write transaction on the bus. Asserting A20M# emulates the 8086 processor's address wrap-around at the 1-Mbyte boundary. Assertion of A20M# is only supported in real mode. A20M# is an asynchronous signal. However, to ensure recognition of this signal following an Input/Output write instruction, it must be valid along with the TRDY# assertion of the corresponding Input/Output Write bus transaction.						
ADS#	Input/ Output	ADS# (Address Strobe) is asserted to indicate the validity of the transaction address on the A[35:3]# and REQ[4:0]# pins. All bus agents observe the ADS# activation to begin parity checking, protocol checking, address decode, internal snoop, or deferred reply ID match operations associated with the new transaction.						
ADSTB[1:0]#	Input/ Output	Address strobes are used to latch A[35:3]# and REQ[4:0]# on their rising and falling edges. Strobes are associated with signals as shown below. <table><tr><th>Signals</th><th>Associated Strobe</th></tr><tr><td>REQ[4:0]#, A[16:3]#</td><td>ADSTB[0]#</td></tr><tr><td>A[35:17]#</td><td>ADSTB[1]#</td></tr></table>	Signals	Associated Strobe	REQ[4:0]#, A[16:3]#	ADSTB[0]#	A[35:17]#	ADSTB[1]#
Signals	Associated Strobe							
REQ[4:0]#, A[16:3]#	ADSTB[0]#							
A[35:17]#	ADSTB[1]#							
BCLK[1:0]	Input	The differential pair BCLK (Bus Clock) determines the FSB frequency. All FSB agents must receive these signals to drive their outputs and latch their inputs. All external timing parameters are specified with respect to the rising edge of BCLK0 crossing V <sub>CROSS</sub> .						
BNR#	Input/ Output	BNR# (Block Next Request) is used to assert a bus stall by any bus agent who is unable to accept new bus transactions. During a bus stall, the current bus owner cannot issue any new transactions.						
BPM[2:1]# BPM[3,0]#	Output  Input/ Output	BPM[3:0]# (Breakpoint Monitor) are breakpoint and performance monitor signals. They are outputs from the processor which indicate the status of breakpoints and programmable counters used for monitoring processor performance. BPM[3:0]# should connect the appropriate pins of all processor FSB agents. This includes debug or performance monitoring tools.						
BPRI#	Input	BPRI# (Bus Priority Request) is used to arbitrate for ownership of the FSB. It must connect the appropriate pins of both FSB agents. Observing BPRI# active (as asserted by the priority agent) causes the other agent to stop issuing new requests, unless such requests are part of an ongoing locked operation. The priority agent keeps BPRI# asserted until all of its requests are completed, then releases the bus by deasserting BPRI#.						
BR0#	Input/ Output	BR0# is used by the processor to request the bus. The arbitration is done between processor (Symmetric Agent) and (G)MCH (High Priority Agent).						

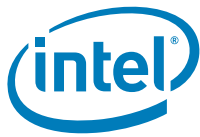


Table 18. Signal Description (Sheet 2 of 7)

Name	Type	Description															
BSEL[2:0]	Output	BSEL[2:0] (Bus Select) are used to select the processor input clock frequency. Table 3 defines the possible combinations of the signals and the frequency associated with each combination. The required frequency is determined by the processor, chipset and clock synthesizer. All agents must operate at the same frequency.															
COMP[3:0]	Analog	COMP[3:0] must be terminated on the system board using precision (1% tolerance) resistors.															
D[63:0]#	Input/ Output	<p>D[63:0]# (Data) are the data signals. These signals provide a 64-bit data path between the FSB agents, and must connect the appropriate pins on both agents. The data driver asserts DRDY# to indicate a valid data transfer.</p> <p>D[63:0]# are quad-pumped signals and are driven four times in a common clock period. D[63:0]# are latched off the falling edge of both DSTBP[3:0]# and DSTBN[3:0]#. Each group of 16 data signals corresponds to a pair of one DSTBP# and one DSTBN#. The following table shows the grouping of data signals to data strobes and DINV#.</p> <p><b>Quad-Pumped Signal Groups</b></p> <table border="1"> <thead> <tr> <th>Data Group</th><th>DSTBN#/ DSTBP#</th><th>DINV#</th></tr> </thead> <tbody> <tr> <td>D[15:0]#</td><td>0</td><td>0</td></tr> <tr> <td>D[31:16]#</td><td>1</td><td>1</td></tr> <tr> <td>D[47:32]#</td><td>2</td><td>2</td></tr> <tr> <td>D[63:48]#</td><td>3</td><td>3</td></tr> </tbody> </table> <p>Furthermore, the DINV# pins determine the polarity of the data signals. Each group of 16 data signals corresponds to one DINV# signal. When the DINV# signal is active, the corresponding data group is inverted and therefore sampled active high.</p>	Data Group	DSTBN#/ DSTBP#	DINV#	D[15:0]#	0	0	D[31:16]#	1	1	D[47:32]#	2	2	D[63:48]#	3	3
Data Group	DSTBN#/ DSTBP#	DINV#															
D[15:0]#	0	0															
D[31:16]#	1	1															
D[47:32]#	2	2															
D[63:48]#	3	3															
DBR#	Output	DBR# (Data Bus Reset) is used only in processor systems where no debug port is implemented on the system board. DBR# is used by a debug port interposer so that an in-target probe can drive system reset. If a debug port is implemented in the system, DBR# is a no-connect in the system. DBR# is not a processor signal.															
DBSY#	Input/ Output	DBSY# (Data Bus Busy) is asserted by the agent responsible for driving data on the FSB to indicate that the data bus is in use. The data bus is released after DBSY# is deasserted. This signal must connect the appropriate pins on both FSB agents.															
DEFER#	Input	DEFER# is asserted by an agent to indicate that a transaction cannot be guaranteed in-order completion. Assertion of DEFER# is normally the responsibility of the addressed memory or Input/Output agent. This signal must connect the appropriate pins of both FSB agents.															



Table 18. Signal Description (Sheet 3 of 7)

Name	Type	Description										
DINV[3:0]#	Input/ Output	<p>DINV[3:0]# (Data Bus Inversion) are source synchronous and indicate the polarity of the D[63:0]# signals. The DINV[3:0]# signals are activated when the data on the data bus is inverted. The bus agent inverts the data bus signals if more than half the bits, within the covered group, would change level in the next cycle.</p> <p><b>DINV[3:0]# Assignment To Data Bus</b></p> <table><tr><th>Bus Signal</th><th>Data Bus Signals</th></tr><tr><td>DINV[3]#</td><td>D[63:48]#</td></tr><tr><td>DINV[2]#</td><td>D[47:32]#</td></tr><tr><td>DINV[1]#</td><td>D[31:16]#</td></tr><tr><td>DINV[0]#</td><td>D[15:0]#</td></tr></table>	Bus Signal	Data Bus Signals	DINV[3]#	D[63:48]#	DINV[2]#	D[47:32]#	DINV[1]#	D[31:16]#	DINV[0]#	D[15:0]#
Bus Signal	Data Bus Signals											
DINV[3]#	D[63:48]#											
DINV[2]#	D[47:32]#											
DINV[1]#	D[31:16]#											
DINV[0]#	D[15:0]#											
DPRSTP#	Input	DPRSTP# when asserted on the platform causes the processor to transition from the Deep Sleep State to the Deeper Sleep state. In order to return to the Deep Sleep State, DPRSTP# must be deasserted. DPRSTP# is driven by the Intel 82801HBM ICH8M I/O Controller Hub based chipset.										
DPSLP#	Input	DPSLP# when asserted on the platform causes the processor to transition from the Sleep State to the Deep Sleep state. In order to return to the Sleep State, DPSLP# must be deasserted. DPSLP# is driven by the Intel 82801HBM ICH8M chipset.										
DPWR#	Input/ Output	DPWR# is a control signal used by the chipset to reduce power on the processor data bus input buffers. The processor drives this pin during dynamic FSB frequency switching.										
DRDY#	Input/ Output	DRDY# (Data Ready) is asserted by the data driver on each data transfer, indicating valid data on the data bus. In a multi-common clock data transfer, DRDY# may be deasserted to insert idle clocks. This signal must connect the appropriate pins of both FSB agents.										
DSTBN[3:0]#	Input/ Output	<p>Data strobe used to latch in D[63:0]#.</p> <table><tr><th>Signals</th><th>Associated Strobe</th></tr><tr><td>D[15:0]#, DINV[0]#</td><td>DSTBN[0]#</td></tr><tr><td>D[31:16]#, DINV[1]#</td><td>DSTBN[1]#</td></tr><tr><td>D[47:32]#, DINV[2]#</td><td>DSTBN[2]#</td></tr><tr><td>D[63:48]#, DINV[3]#</td><td>DSTBN[3]#</td></tr></table>	Signals	Associated Strobe	D[15:0]#, DINV[0]#	DSTBN[0]#	D[31:16]#, DINV[1]#	DSTBN[1]#	D[47:32]#, DINV[2]#	DSTBN[2]#	D[63:48]#, DINV[3]#	DSTBN[3]#
Signals	Associated Strobe											
D[15:0]#, DINV[0]#	DSTBN[0]#											
D[31:16]#, DINV[1]#	DSTBN[1]#											
D[47:32]#, DINV[2]#	DSTBN[2]#											
D[63:48]#, DINV[3]#	DSTBN[3]#											
DSTBP[3:0]#	Input/ Output	<p>Data strobe used to latch in D[63:0]#.</p> <table><tr><th>Signals</th><th>Associated Strobe</th></tr><tr><td>D[15:0]#, DINV[0]#</td><td>DSTBP[0]#</td></tr><tr><td>D[31:16]#, DINV[1]#</td><td>DSTBP[1]#</td></tr><tr><td>D[47:32]#, DINV[2]#</td><td>DSTBP[2]#</td></tr><tr><td>D[63:48]#, DINV[3]#</td><td>DSTBP[3]#</td></tr></table>	Signals	Associated Strobe	D[15:0]#, DINV[0]#	DSTBP[0]#	D[31:16]#, DINV[1]#	DSTBP[1]#	D[47:32]#, DINV[2]#	DSTBP[2]#	D[63:48]#, DINV[3]#	DSTBP[3]#
Signals	Associated Strobe											
D[15:0]#, DINV[0]#	DSTBP[0]#											
D[31:16]#, DINV[1]#	DSTBP[1]#											
D[47:32]#, DINV[2]#	DSTBP[2]#											
D[63:48]#, DINV[3]#	DSTBP[3]#											



Table 18. Signal Description (Sheet 4 of 7)

Name	Type	Description
FERR#/PBE#	Output	<p>FERR# (Floating-point Error)/PBE#(Pending Break Event) is a multiplexed signal and its meaning is qualified with STPCLK#. When STPCLK# is not asserted, FERR#/PBE# indicates a floating point when the processor detects an unmasked floating-point error. FERR# is similar to the ERROR# signal on the Intel 387 coprocessor, and is included for compatibility with systems using MS-DOS*-type floating-point error reporting. When STPCLK# is asserted, an assertion of FERR#/PBE# indicates that the processor has a pending break event waiting for service. The assertion of FERR#/PBE# indicates that the processor should be returned to the Normal state. When FERR#/PBE# is asserted, indicating a break event, it remains asserted until STPCLK# is deasserted. Assertion of PREQ# when STPCLK# is active also causes an FERR# break event.</p> <p>For additional information on the pending break event functionality, including identification of support of the feature and enable/disable information, refer to Volumes 3A and 3B of the <i>Intel® 64 and IA-32 Architectures Software Developer's Manual</i> and the <i>Intel® Processor Identification and CPUID Instruction</i> application note.</p>
GTLREF	Input	<p>GTLREF determines the signal reference level for AGTL+ input pins. GTLREF should be set at <math>2/3 V_{CCP}</math>. GTLREF is used by the AGTL+ receivers to determine if a signal is a logical 0 or logical 1.</p>
HIT# HITM#	Input/ Output Input/ Output	<p>HIT# (Snoop Hit) and HITM# (Hit Modified) convey transaction snoop operation results. Either FSB agent may assert both HIT# and HITM# together to indicate that it requires a snoop stall, which can be continued by reasserting HIT# and HITM# together.</p>
IERR#	Output	<p>IERR# (Internal Error) is asserted by a processor as the result of an internal error. Assertion of IERR# is usually accompanied by a SHUTDOWN transaction on the FSB. This transaction may optionally be converted to an external error signal (e.g., NMI) by system core logic. The processor keeps IERR# asserted until the assertion of RESET#, BINIT#, or INIT#.</p>
IGNNE#	Input	<p>IGNNE# (Ignore Numeric Error) is asserted to force the processor to ignore a numeric error and continue to execute noncontrol floating-point instructions. If IGNNE# is deasserted, the processor generates an exception on a noncontrol floating-point instruction if a previous floating-point instruction caused an error. IGNNE# has no effect when the NE bit in control register 0 (CRO) is set.</p> <p>IGNNE# is an asynchronous signal. However, to ensure recognition of this signal following an Input/Output write instruction, it must be valid along with the TRDY# assertion of the corresponding Input/Output Write bus transaction.</p>
INIT#	Input	<p>INIT# (Initialization), when asserted, resets integer registers inside the processor without affecting its internal caches or floating-point registers. The processor then begins execution at the power-on Reset vector configured during power-on configuration. The processor continues to handle snoop requests during INIT# assertion. INIT# is an asynchronous signal. However, to ensure recognition of this signal following an Input/Output Write instruction, it must be valid along with the TRDY# assertion of the corresponding Input/Output Write bus transaction. INIT# must connect the appropriate pins of both FSB agents.</p> <p>If INIT# is sampled active on the active to inactive transition of RESET#, then the processor executes its Built-in Self-Test (BIST)</p>





Table 18. Signal Description (Sheet 5 of 7)

Name	Type	Description
LINT[1:0]	Input	<p>LINT[1:0] (Local APIC Interrupt) must connect the appropriate pins of all APIC Bus agents. When the APIC is disabled, the LINT0 signal becomes INTR, a maskable interrupt request signal, and LINT1 becomes NMI, a nonmaskable interrupt. INTR and NMI are backward compatible with the signals of those names on the Intel® Pentium® processor. Both signals are asynchronous.</p> <p>Both of these signals must be software configured via BIOS programming of the APIC register space to be used either as NMI/INTR or LINT[1:0]. Because the APIC is enabled by default after Reset, operation of these pins as LINT[1:0] is the default configuration.</p>
LOCK#	Input/ Output	<p>LOCK# indicates to the system that a transaction must occur atomically. This signal must connect the appropriate pins of both FSB agents. For a locked sequence of transactions, LOCK# is asserted from the beginning of the first transaction to the end of the last transaction.</p> <p>When the priority agent asserts BPRI# to arbitrate for ownership of the FSB, it waits until it observes LOCK# deasserted. This enables symmetric agents to retain ownership of the FSB throughout the bus locked operation and ensure the atomicity of lock.</p>
PRDY#	Output	Probe Ready signal used by debug tools to determine processor debug readiness.
PREQ#	Input	Probe Request signal used by debug tools to request debug operation of the processor.
PROCHOT#	Input/ Output	<p>As an output, PROCHOT# (Processor Hot) goes active when the processor temperature monitoring sensor detects that the processor has reached its maximum safe operating temperature. This indicates that the processor Thermal Control Circuit (TCC) has been activated, if enabled. As an input, assertion of PROCHOT# by the system activates the TCC, if enabled. The TCC remains active until the system deasserts PROCHOT#.</p> <p>By default PROCHOT# is configured as an output. The processor must be enabled via the BIOS for PROCHOT# to be configured as bidirectional.</p> <p>This signal may require voltage translation on the motherboard.</p>
PSI#	Output	Processor Power Status Indicator signal. This signal is asserted when the processor is in both in the Normal state (HFM to LFM) and in lower power states (Deep Sleep and Deeper Sleep).
PWRGOOD	Input	<p>PWRGOOD (Power Good) is a processor input. The processor requires this signal to be a clean indication that the clocks and power supplies are stable and within their specifications. 'Clean' implies that the signal remains low (capable of sinking leakage current), without glitches, from the time that the power supplies are turned on until they come within specification. The signal must then transition monotonically to a high state. PWRGOOD can be driven inactive at any time, but clocks and power must again be stable before a subsequent rising edge of PWRGOOD.</p> <p>The PWRGOOD signal must be supplied to the processor; it is used to protect internal circuits against voltage sequencing issues. It should be driven high throughout boundary scan operation.</p>
REQ[4:0]#	Input/ Output	REQ[4:0]# (Request Command) must connect the appropriate pins of both FSB agents. They are asserted by the current bus owner to define the currently active transaction type. These signals are source synchronous to ADSTB[0]#.



Table 18. Signal Description (Sheet 6 of 7)

Name	Type	Description
RESET#	Input	Asserting the RESET# signal resets the processor to a known state and invalidates its internal caches without writing back any of their contents. For a power-on Reset, RESET# must stay active for at least two milliseconds after V <sub>CC</sub> and BCLK have reached their proper specifications. On observing active RESET#, both FSB agents deasserts their outputs within two clocks. All processor straps must be valid within the specified setup time before RESET# is deasserted. There is a 55-Ω (nominal) on die pull-up resistor on this signal.
RS[2:0]#	Input	RS[2:0]# (Response Status) are driven by the response agent (the agent responsible for completion of the current transaction), and must connect the appropriate pins of both FSB agents.
RSVD	Reserved /No Connect	These pins are RESERVED and must be left unconnected on the board. However, it is recommended that routing channels to these pins on the board be kept open for possible future use.
SLP#	Input	SLP# (Sleep), when asserted in Stop-Grant state, causes the processor to enter the Sleep state. During Sleep state, the processor stops providing internal clock signals to all units, leaving only the Phase-Locked Loop (PLL) still operating. Processors in this state does not recognize snoops or interrupts. The processor recognizes only assertion of the RESET# signal, deassertion of SLP#, and removal of the BCLK input while in Sleep state. If SLP# is deasserted, the processor exits Sleep state and returns to Stop-Grant state, restarting its internal clock signals to the bus and processor core units. If DPSLP# is asserted while in the Sleep state, the processor exits the Sleep state and transition to the Deep Sleep state.
SMI#	Input	SMI# (System Management Interrupt) is asserted asynchronously by system logic. On accepting a System Management Interrupt, the processor saves the current state and enters System Management Mode (SMM). An SMI Acknowledge transaction is issued and the processor begins program execution from the SMM handler. If an SMI# is asserted during the deassertion of RESET#, then the processor tristates its outputs.
STPCLK#	Input	STPCLK# (Stop Clock), when asserted, causes the processor to enter a low power Stop-Grant state. The processor issues a Stop-Grant Acknowledge transaction, and stops providing internal clock signals to all processor core units except the FSB and APIC units. The processor continues to snoop bus transactions and service interrupts while in Stop-Grant state. When STPCLK# is deasserted, the processor restarts its internal clock to all units and resumes execution. The assertion of STPCLK# has no effect on the bus clock; STPCLK# is an asynchronous input.
TCK	Input	TCK (Test Clock) provides the clock input for the processor Test Bus (also known as the Test Access Port).
TDI	Input	TDI (Test Data In) transfers serial test data into the processor. TDI provides the serial input needed for JTAG specification support.
TDO	Output	TDO (Test Data Out) transfers serial test data out of the processor. TDO provides the serial output needed for JTAG specification support.
TEST1, TEST2, TEST3, TEST4, TEST5, TEST6	Input	TEST1 and TEST2 must have a stuffing option of separate pulldown resistors to V <sub>SS</sub> . For the purpose of testability, route the TEST3 and TEST5 signals through a ground-referenced Zo=55 ohm trace that ends in a via that is near a GND via and is accessible through an oscilloscope connection.
THRMDA	Other	Thermal Diode Anode.
THRMDC	Other	Thermal Diode Cathode.



Table 18. Signal Description (Sheet 7 of 7)

Name	Type	Description
THERMTRIP#	Output	The processor protects itself from catastrophic overheating by use of an internal thermal sensor. This sensor is set well above the normal operating temperature to ensure that there are no false trips. The processor stops all execution when the junction temperature exceeds approximately 125°C. This is signalled to the system by the THERMTRIP# (Thermal Trip) pin.
TMS	Input	TMS (Test Mode Select) is a JTAG specification support signal used by debug tools.
TRDY#	Input	TRDY# (Target Ready) is asserted by the target to indicate that it is ready to receive a write or implicit writeback data transfer. TRDY# must connect the appropriate pins of both FSB agents.
TRST#	Input	TRST# (Test Reset) resets the Test Access Port (TAP) logic. TRST# must be driven low during power on Reset.
V <sub>CC</sub>	Input	Processor core power supply.
V <sub>SS</sub>	Input	Processor core ground node.
V <sub>CCA</sub>	Input	V <sub>CCA</sub> provides isolated power for the internal processor core PLL's.
V <sub>CCP</sub>	Input	Processor I/O Power Supply.
V <sub>CC_SENSE</sub>	Output	V <sub>CC_SENSE</sub> together with V <sub>SS_SENSE</sub> are voltage feedback signals to Intel MVP-6 that control the 2.1-mΩ loadline at the processor die. It should be used to sense voltage near the silicon with little noise.
VID[6:0]	Output	VID[6:0] (Voltage ID) pins are used to support automatic selection of power supply voltages (V <sub>CC</sub> ). Unlike some previous generations of processors, these are CMOS signals that are driven by the processor. The voltage supply for these pins must be valid before the VR can supply V <sub>CC</sub> to the processor. Conversely, the VR output must be disabled until the voltage supply for the VID pins becomes valid. The VID pins are needed to support the processor voltage specification variations. See <a href="#">Table 2</a> for definitions of these pins. The VR must supply the voltage that is requested by the pins, or disable itself.
V <sub>SS_SENSE</sub>	Output	V <sub>SS_SENSE</sub> together with V <sub>CC_SENSE</sub> are voltage feedback signals to Intel MVP-6 that control the 2.1-mΩ loadline at the processor die. It should be used to sense ground near the silicon with little noise.





## 5 Thermal Specifications and Design Considerations

Maintaining the proper thermal environment is key to reliable, long-term system operation. A complete thermal solution includes both component and system level thermal management features. The system/processor thermal solution should be designed so that the processor remains within the minimum and maximum junction temperature ( $T_J$ ) specifications at the corresponding thermal design power (TDP) value listed in [Table 19](#) through [Table 20](#).

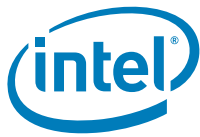
**Caution:** Operating the processor outside these limits may result in permanent damage to the processor and potentially other components in the system.

**Table 19. Power Specifications for the Intel Core 2 Duo Processor - Standard Voltage**

Symbol	Processor Number	Core Frequency & Voltage	Thermal Design Power			Unit	Notes
TDP	T7800	2.6 GHz & HFM V <sub>CC</sub>	35			W	1, 4, 5, 6, 9 1, 4, 5, 6, 9 1, 4, 5, 6, 9 1, 4, 5, 6, 10
	T7700	2.4 GHz & HFM V <sub>CC</sub>	35				
	T7500	2.2 GHz & HFM V <sub>CC</sub>	35				
	T7300	2.0 GHz & HFM V <sub>CC</sub>	35				
	T7250	2.0 GHz & HFM V <sub>CC</sub>	35				
	T7100	1.8 GHz & HFM V <sub>CC</sub>	35				
		1.2 GHz & LFM V <sub>CC</sub>	25				
		0.80 GHZ & SuperLFM V <sub>CC</sub>	12				
Symbol	Parameter		Min	Typ	Max	Unit	
P <sub>AH</sub> , P <sub>SGNT</sub>	Auto Halt, Stop Grant Power at HFM V <sub>CC</sub> at SuperLFM V <sub>CC</sub>				13.5 6.9	W	2, 5, 7
P <sub>SLP</sub>	Sleep Power at HFM V <sub>CC</sub> at SuperLFM V <sub>CC</sub>				12.9 6.7	W	2, 5, 7
P <sub>DSLP</sub>	Deep Sleep Power at HFM V <sub>CC</sub> at SuperLFM V <sub>CC</sub>				7.7 4.3	W	2, 5, 8
P <sub>DPRSLP</sub>	Deeper Sleep Power				2.0	W	2, 8
P <sub>DC4</sub>	Intel® Enhanced Deeper Sleep Power				1.2	W	2, 8
T <sub>J</sub>	Junction Temperature		0		100	°C	3, 4

### NOTES:

1. The TDP specification should be used to design the processor thermal solution. The TDP is not the maximum theoretical power the processor can generate.
2. Not 100% tested. These power specifications are determined by characterization of the processor currents at higher temperatures and extrapolating the values for the temperature indicated.
3. As measured by the activation of the on-die Intel Thermal Monitor. The Intel Thermal Monitor's automatic mode is used to indicate that the maximum  $T_J$  has been reached. Refer to [Section 5.1](#) for details.
4. The Intel Thermal Monitor automatic mode must be enabled for the processor to operate within specifications.



5. Processor TDP requirements in Intel Dynamic Acceleration Technology mode is lesser than TDP in HFM.
6. At  $T_J$  of 100°C
7. At  $T_J$  of 50°C
8. At  $T_J$  of 35°C
9. 4-M L2 cache
10. 2-M L2 cache

**Table 20. Power Specifications for the Intel Core 2 Duo Processor - Low Voltage**

Symbol	Processor Number	Core Frequency & Voltage	Thermal Design Power			Unit	Notes
TDP	L7700	1.8 GHz & HFM V <sub>CC</sub>	17			W	1, 4, 5, 6, 9
	L7500	1.6 GHz & HFM V <sub>CC</sub>	17				
	L7300	1.4 GHz & HFM V <sub>CC</sub>	17				
		1.2 GHz & LFM V <sub>CC</sub>	16.1				
		0.80 GHz & SuperLFM V <sub>CC</sub>	10.0				
Symbol	Parameter		Min	Typ	Max	Unit	
P <sub>AH</sub> , P <sub>SGNT</sub>	Auto Halt, Stop Grant Power at HFM V <sub>CC</sub> at SuperLFM V <sub>CC</sub>				5.6 3.9	W	2, 5, 7
P <sub>SLP</sub>	Sleep Power at HFM V <sub>CC</sub> at SuperLFM V <sub>CC</sub>				5.3 3.6	W	2, 5, 7
P <sub>DSLP</sub>	Deep Sleep Power at HFM V <sub>CC</sub> at SuperLFM V <sub>CC</sub>				2.8 2.3	W	2, 5, 8
P <sub>DPRSLP</sub>	Deeper Sleep Power				1.3	W	2, 8
P <sub>DC4</sub>	Intel® Enhanced Deeper Sleep Power				0.8	W	2, 8
T <sub>J</sub>	Junction Temperature		0		100	°C	3, 4

**NOTES:**

1. The TDP specification should be used to design the processor thermal solution. The TDP is not the maximum theoretical power the processor can generate.
2. Not 100% tested. These power specifications are determined by characterization of the processor currents at higher temperatures and extrapolating the values for the temperature indicated.
3. As measured by the activation of the on-die Intel Thermal Monitor. The Intel Thermal Monitor's automatic mode is used to indicate that the maximum  $T_J$  has been reached. Refer to [Section 5.1](#) for more details.
4. The Intel Thermal Monitor automatic mode must be enabled for the processor to operate within specifications.
5. Processor TDP requirements in Intel Dynamic Acceleration Technology mode is lesser than TDP in HFM.
6. At  $T_J$  of 100°C.
7. At  $T_J$  of 50°C.
8. At  $T_J$  of 35°C.
9. 4-M L2 cache.

**Table 21. Power Specifications for the Intel Core 2 Duo Processor - Ultra Low Voltage**

Symbol	Processor Number	Core Frequency & Voltage	Thermal Design Power			Unit	Notes
TDP	U7700	1.33 GHz & HFM V <sub>CC</sub>	10			W	1, 4, 5, 6, 9
	U7600	1.20 GHz & HFM V <sub>CC</sub>	10				
	U7500	1.06 GHz & HFM V <sub>CC</sub>	10				
		0.80 GHZ & LFM V <sub>CC</sub>	9.2				
Symbol	Parameter		Min	Typ	Max	Unit	
P <sub>AH</sub> , P <sub>SGNT</sub>	Auto Halt, Stop Grant Power at HFM V <sub>CC</sub> at LFM V <sub>CC</sub>				3.1 2.6	W	2, 5, 7
P <sub>SLP</sub>	Sleep Power at HFM V <sub>CC</sub> at LFM V <sub>CC</sub>				3.0 2.5	W	2, 5, 7
P <sub>DSLP</sub>	Deep Sleep Power at HFM V <sub>CC</sub> at LFM V <sub>CC</sub>				1.5 1.3	W	2, 5, 8
P <sub>DPRSLP</sub>	Deeper Sleep Power				1.0	W	2, 8
P <sub>DC4</sub>	Intel Enhanced Deeper Sleep Power				0.7	W	2, 8
T <sub>J</sub>	Junction Temperature		0		100	°C	3, 4

**NOTES:**

1. The TDP specification should be used to design the processor thermal solution. The TDP is not the maximum theoretical power the processor can generate.
2. Not 100% tested. These power specifications are determined by characterization of the processor currents at higher temperatures and extrapolating the values for the temperature indicated.
3. As measured by the activation of the on-die Intel Thermal Monitor. The Intel Thermal Monitor's automatic mode is used to indicate that the maximum  $T_J$  has been reached. Refer to [Section 5.1](#) for more details.
4. The Intel Thermal Monitor automatic mode must be enabled for the processor to operate within specifications.
5. Processor TDP requirements in Intel Dynamic Acceleration Technology mode is lesser than TDP in HFM.
6. At  $T_J$  of 100°C.
7. At  $T_J$  of 50°C.
8. At  $T_J$  of 35°C.
9. 2-M L2 cache.



**Table 22. Power Specifications for the Intel Core 2 Extreme Processor**

Symbol	Processor Number	Core Frequency & Voltage	Thermal Design Power			Unit	Notes
TDP	X7900 X7800	2.8 GHz & HFM V <sub>CC</sub>	44			W	1, 4, 5, 6, 9
		2.6 GHz & HFM V <sub>CC</sub>	44				
		1.2 GHz & LFM V <sub>CC</sub>	35				
		0.80 GHz & SuperLFM V <sub>CC</sub>	27				
Symbol	Parameter		Min	Typ	Max	Unit	
P <sub>AH</sub> , P <sub>SGNT</sub>	Auto Halt, Stop Grant Power at HFM V <sub>CC</sub> at SuperLFM V <sub>CC</sub>				15.7 9.3	W	2, 5, 7
P <sub>SLP</sub>	Sleep Power at HFM V <sub>CC</sub> at SuperLFM V <sub>CC</sub>				15.0 9.1	W	2, 5, 7
P <sub>DSLP</sub>	Deep Sleep Power at HFM V <sub>CC</sub> at SuperLFM V <sub>CC</sub>				9.5 6.0	W	2, 5, 8
P <sub>DPRSLP</sub>	Deeper Sleep Power				3.0	W	2, 8
P <sub>DC4</sub>	Intel Enhanced Deeper Sleep Power				2.5	W	2, 8
T <sub>J</sub>	Junction Temperature		0		100	°C	3, 4

**NOTES:**

1. The TDP specification should be used to design the processor thermal solution. The TDP is not the maximum theoretical power the processor can generate.
2. Not 100% tested. These power specifications are determined by characterization of the processor currents at higher temperatures and extrapolating the values for the temperature indicated.
3. As measured by the activation of the on-die Intel Thermal Monitor. The Intel Thermal Monitor's automatic mode is used to indicate that the maximum  $T_J$  has been reached. Refer to [Section 5.1](#) for more details.
4. The Intel Thermal Monitor automatic mode must be enabled for the processor to operate within specifications.
5. Intel Dynamic Acceleration mode is not supported.
6. At  $T_J$  of 100°C.
7. At  $T_J$  of 50°C.
8. At  $T_J$  of 35°C.
9. 4-M L2 cache.

## 5.1 Thermal Specifications

The processor incorporates three methods of monitoring die temperature:

- Thermal Diode
- Intel Thermal Monitor
- Digital Thermal Sensor





### 5.1.1 Thermal Diode

The processor incorporates an on-die PNP transistor whose base emitter junction is used as a thermal diode, with its collector shorted to ground. The thermal diode can be read by an off-die analog/digital converter (a thermal sensor) located on the motherboard or a stand-alone measurement kit. The thermal diode may be used to monitor the die temperature of the processor for thermal management or instrumentation purposes but is not a reliable indication that the maximum operating temperature of the processor has been reached. When using the thermal diode, a temperature offset value must be read from a processor MSR and applied. See [Section 5.1.2](#) for more details. Please see [Section 5.1.3](#) for thermal diode usage recommendation when the PROCHOT# signal is not asserted.

**The reading of the external thermal sensor (on the motherboard) connected to the processor thermal diode signals does not reflect the temperature of the hottest location on the die.** This is due to inaccuracies in the external thermal sensor, on-die temperature gradients between the location of the thermal diode and the hottest location on the die, and time based variations in the die temperature measurement. Time-based variations can occur when the sampling rate of the thermal diode (by the thermal sensor) is slower than the rate at which the  $T_j$  temperature can change.

Offset between the thermal diode-based temperature reading and the Intel Thermal Monitor reading may be characterized using the Intel Thermal Monitor's Automatic mode activation of the thermal control circuit. This temperature offset must be taken into account when using the processor thermal diode to implement power management events. This offset is different than the diode Toffset value programmed into the processor Model Specific Register (MSR).

[Table 23](#) to [Table 26](#) provide the diode interface and specifications. The diode model parameters apply to the traditional thermal sensors that use the diode equation to determine the processor temperature. Transistor model parameters have been added to support thermal sensors that use the transistor equation method. The Transistor model may provide more accurate temperature measurements when the diode ideality factor is closer to the maximum or minimum limits. Contact your external sensor supplier for recommendations. The thermal diode is separate from the Intel Thermal Monitor's thermal sensor and cannot be used to predict the behavior of the Intel Thermal Monitor.

**Table 23. Thermal Diode Interface**

Signal Name	Pin/Ball Number	Signal Description
THERMDA	A24	Thermal diode anode
THERMDC	A25	Thermal diode cathode



Table 24. Thermal Diode Parameters Using Diode Model

Symbol	Parameter	Min	Typ	Max	Unit	Notes
$I_{FW}$	Forward Bias Current	5		200	$\mu A$	1
$n$	Diode Ideality Factor	1.000	1.009	1.050		2, 3, 4
$R_T$	Series Resistance	2.79	4.52	6.24	$\Omega$	2, 3, 5

**NOTES:**

- Intel does not support or recommend operation of the thermal diode under reverse bias. Intel does not support or recommend operation of the thermal diode when the processor power supplies are not within their specified tolerance range.
- Characterized across a temperature range of 50-100°C.
- Not 100% tested. Specified by design characterization.
- The ideality factor,  $n$ , represents the deviation from ideal diode behavior as exemplified by the diode equation:

$$I_{FW} = I_S * (e^{qV_D/nkT} - 1)$$

where  $I_S$  = saturation current,  $q$  = electronic charge,  $V_D$  = voltage across the diode,  $k$  = Boltzmann Constant, and  $T$  = absolute temperature (Kelvin).

- The series resistance,  $R_T$ , is provided to allow for a more accurate measurement of the junction temperature.  $R_T$ , as defined, includes the lands of the processor but does not include any socket resistance or board trace resistance between the socket and the external remote diode thermal sensor.  $R_T$  can be used by remote diode thermal sensors with automatic series resistance cancellation to calibrate out this error term. Another application is that a temperature offset can be manually calculated and programmed into an offset register in the remote diode thermal sensors as exemplified by the equation:

$$T_{error} = [R_T * (N-1) * I_{FWmin}] / [nk/q * \ln N]$$

where  $T_{error}$  = sensor temperature error,  $N$  = sensor current ratio,  $k$  = Boltzmann Constant,  $q$  = electronic charge.

**Table 25. Thermal Diode Parameters Using Transistor Model**

Symbol	Parameter	Min	Typ	Max	Unit	Notes
$I_{FW}$	Forward Bias Current	5		200	$\mu A$	1,2
$I_E$	Emitter Current	5		200	$\mu A$	1
$n_Q$	Transistor Ideality	0.997	1.001	1.005		3,4,5
Beta		0.3		0.760		3,4
$R_T$	Series Resistance	2.79	4.52	6.24	$\Omega$	3,6

**NOTES:**

1. Intel does not support or recommend operation of the thermal diode under reverse bias.
2. Same as  $I_{FW}$  in [Table 24](#).
3. Characterized across a temperature range of 50-100°C.
4. Not 100% tested. Specified by design characterization.
5. The ideality factor,  $n_Q$ , represents the deviation from ideal transistor model behavior as exemplified by the equation for the collector current:

$$I_C = I_S * (e^{qV_{BE}/n_QkT} - 1)$$

where  $I_S$  = saturation current,  $q$  = electronic charge,  $V_{BE}$  = voltage across the transistor base emitter junction (same nodes as VD),  $k$  = Boltzmann Constant, and  $T$  = absolute temperature (Kelvin).

6. The series resistance,  $R_T$ , provided in the Diode Model Table ([Table 24](#)) can be used for more accurate readings as needed.

When calculating a temperature based on the thermal diode measurements, a number of parameters must be either measured or assumed. Most devices measure the diode ideality and assume a series resistance and ideality trim value, although are capable of also measuring the series resistance. Calculating the temperature is then accomplished using the equations listed under [Table 24](#). In most sensing devices, an expected value for the diode ideality is designed-in to the temperature calculation equation. If the designer of the temperature sensing device assumes a perfect diode, the ideality value (also called  $n_{trim}$ ) is 1.000. Given that most diodes are not perfect, the designers usually select an  $n_{trim}$  value that more closely matches the behavior of the diodes in the processor. If the processor diode ideality deviates from that of the  $n_{trim}$ , each calculated temperature offsets by a fixed amount. This temperature offset can be calculated with the equation:

$$T_{error(nf)} = T_{measured} * (1 - n_{actual}/n_{trim})$$

where  $T_{error(nf)}$  is the offset in degrees C,  $T_{measured}$  is in Kelvin,  $n_{actual}$  is the measured ideality of the diode, and  $n_{trim}$  is the diode ideality assumed by the temperature sensing device.

### 5.1.2 Thermal Diode Offset

In order to improve the accuracy of the diode-based temperature measurements, a temperature offset value (specified as  $T_{offset}$ ) is programmed in the processor MSR which contains thermal diode characterization data. During manufacturing each processor thermal diode is evaluated for its behavior relative to the theoretical diode. Using the equation above, the temperature error created by the difference  $n_{trim}$  and the actual ideality of the particular processor is calculated.



If the  $n_{\text{trim}}$  value used to calculate the Toffset differs from the  $n_{\text{trim}}$  value used to in a temperature sensing device, the  $T_{\text{error(nf)}}$  may not be accurate. If desired, the Toffset can be adjusted by calculating  $n_{\text{actual}}$  and then recalculating the offset using the  $n_{\text{trim}}$  as defined in the temperature sensor manufacturer's datasheet.

The  $n_{\text{trim}}$  used to calculate the Diode Correction Toffset are listed in [Table 26](#).

**Table 26. Thermal Diode  $n_{\text{trim}}$  and Diode Correction Toffset**

Symbol	Parameter	Value
$n_{\text{trim}}$	Diode Ideality used to calculate Toffset	1.01

### 5.1.3 Intel® Thermal Monitor

The Intel Thermal Monitor helps control the processor temperature by activating the TCC (Thermal Control Circuit) when the processor silicon reaches its maximum operating temperature. The temperature at which the Intel Thermal Monitor activates the TCC is not user configurable. Bus traffic is snooped in the normal manner and interrupt requests are latched (and serviced during the time that the clocks are on) while the TCC is active.

With a properly designed and characterized thermal solution, it is anticipated that the TCC would only be activated for very short periods of time when running the most power intensive applications. The processor performance impact due to these brief periods of TCC activation is expected to be minor and hence not detectable. An under-designed thermal solution that is not able to prevent excessive activation of the TCC in the anticipated ambient environment may cause a noticeable performance loss and may affect the long-term reliability of the processor. In addition, a thermal solution that is significantly under-designed may not be capable of cooling the processor even when the TCC is active continuously.

The Intel Thermal Monitor controls the processor temperature by modulating (starting and stopping) the processor core clocks or by initiating an Enhanced Intel SpeedStep Technology transition when the processor silicon reaches its maximum operating temperature. The Intel Thermal Monitor uses two modes to activate the TCC: automatic mode and on-demand mode. If both modes are activated, automatic mode takes precedence.

There are two automatic modes called Intel Thermal Monitor 1 and Intel Thermal Monitor 2. These modes are selected by writing values to the MSRs of the processor. After automatic mode is enabled, the TCC activates only when the internal die temperature reaches the maximum allowed value for operation.

When Intel Thermal Monitor 1 is enabled and a high temperature situation exists, the clocks modulates by alternately turning the clocks off and on at a 50% duty cycle. Cycle times are processor speed dependent and decreases linearly as processor core frequencies increase. Once the temperature has returned to a non-critical level, modulation ceases and TCC goes inactive. A small amount of hysteresis has been included to prevent rapid active/inactive transitions of the TCC when the processor temperature is near the trip point. The duty cycle is factory configured and cannot be modified. Also, automatic mode does not require any additional hardware, software drivers, or interrupt handling routines. Processor performance decreases by the same amount as the duty cycle when the TCC is active.

When Intel Thermal Monitor 2 is enabled and a high temperature situation exists, the processor performs an Enhanced Intel SpeedStep Technology transition to the LFM. When the processor temperature drops below the critical level, the processor makes an Enhanced Intel SpeedStep Technology transition to the last requested operating point. The processor also supports Enhanced Multi Threaded Thermal Monitoring (EMTTM).



EMTTM is a processor feature that enhances Intel Thermal Monitor 2 with a processor throttling algorithm known as Adaptive Intel Thermal Monitor 2. Adaptive Intel Thermal Monitor 2 transitions to intermediate operating points, rather than directly to the LFM, once the processor has reached its thermal limit and subsequently searches for the highest possible operating point. Please ensure this feature is enabled and supported in the BIOS. Also with EMTTM enabled, the operating system can request the processor to throttling to any point between Intel Dynamic Acceleration Technology frequency and SuperLFM frequency as long as these features are enabled in the BIOS and supported by the processor. The Intel Thermal Monitor automatic mode and Enhanced Multi Threaded Thermal Monitoring must be enabled through BIOS for the processor to be operating within specifications.

**Note:** Intel Thermal Monitor 1, Intel Thermal Monitor 2 and EMTTM features are collectively referred to as Adaptive Thermal Monitoring features. Intel recommends Intel Thermal Monitor 1 and 2 be enabled on the processors.

Intel Thermal Monitor 1 and 2 can co-exist within the processor. If both Intel Thermal Monitor 1 and 2 bits are enabled in the auto-throttle MSR, Intel Thermal Monitor 2 takes precedence over Intel Thermal Monitor 1. However, if Force Intel Thermal Monitor 1 over Intel Thermal Monitor 2 is enabled in MSRs via BIOS and Intel Thermal Monitor 2 is not sufficient to cool the processor below the maximum operating temperature, then Intel Thermal Monitor 1 also activates to help cool down the processor.

If a processor load based Enhanced Intel SpeedStep Technology transition (through MSR write) is initiated when a Intel Thermal Monitor 2 period is active, there are two possible results:

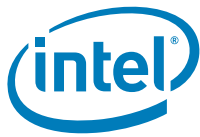
1. If the processor load based Enhanced Intel SpeedStep Technology transition target frequency is **higher** than the Intel Thermal Monitor 2 transition-based target frequency, the processor load-based transition defers until the Intel Thermal Monitor 2 event has been completed.
2. If the processor load-based Enhanced Intel SpeedStep Technology transition target frequency is **lower** than the Intel Thermal Monitor 2 transition-based target frequency, the processor transitions to the processor load-based Enhanced Intel SpeedStep Technology target frequency point.

The TCC may also be activated via on-demand mode. If bit 4 of the ACPI Intel Thermal Monitor control register is written to a 1, the TCC activates immediately independent of the processor temperature. When using on-demand mode to activate the TCC, the duty cycle of the clock modulation is programmable via bits 3:1 of the same ACPI Intel Thermal Monitor control register. In automatic mode, the duty cycle is fixed at 50% on, 50% off, however in on-demand mode, the duty cycle can be programmed from 12.5% on/ 87.5% off, to 87.5% on/12.5% off in 12.5% increments. On-demand mode may be used at the same time automatic mode is enabled, however, if the system tries to enable the TCC via on-demand mode at the same time automatic mode is enabled and a high temperature condition exists, automatic mode takes precedence.

An external signal, PROCHOT# (processor hot) is asserted when the processor detects that its temperature is above the thermal trip point. Bus snooping and interrupt latching are also active while the TCC is active.

Besides the thermal sensor and thermal control circuit, the Intel Thermal Monitor also includes one ACPI register, one performance counter register, three MSR, and one I/O pin (PROCHOT#). All are available to monitor and control the state of the Intel Thermal Monitor feature. The Intel Thermal Monitor can be configured to generate an interrupt upon the assertion or deassertion of PROCHOT#.

PROCHOT# is not be asserted when the processor is in the Stop Grant, Sleep, Deep Sleep, and Deeper Sleep low power states, hence the thermal diode reading must be used as a safeguard to maintain the processor junction temperature within maximum specification. If the platform thermal solution is not able to maintain the processor



junction temperature within the maximum specification, the system must initiate an orderly shutdown to prevent damage. If the processor enters one of the above low power states with PROCHOT# already asserted, PROCHOT# will remain asserted until the processor exits the low power state and the processor junction temperature drops below the thermal trip point.

If Intel Thermal Monitor automatic mode is disabled, the processor will be operating out of specification. Regardless of enabling the automatic or on-demand modes, in the event of a catastrophic cooling failure, the processor will automatically shut down when the silicon has reached a temperature of approximately 125°C. At this point the THERMTRIP# signal will go active. THERMTRIP# activation is independent of processor activity and does not generate any bus cycles. When THERMTRIP# is asserted, the processor core voltage must be shut down within the time specified in [Chapter 3](#).

In all cases the Intel Thermal Monitor feature must be enabled for the processor to remain within specification.

#### 5.1.4 Digital Thermal Sensor

The processor also contains an on die Digital Thermal Sensor (DTS) that can be read via an MSR (no I/O interface). Each core of the processor will have a unique digital thermal sensor whose temperature is accessible via the processor MSRs. The DTS is the preferred method of reading the processor die temperature since it can be located much closer to the hottest portions of the die and can thus more accurately track the die temperature and potential activation of processor core clock modulation via the Intel Thermal Monitor. The DTS is only valid while the processor is in the normal operating state (the Normal package level low power state).

Unlike traditional thermal devices, the DTS will output a temperature relative to the maximum supported operating temperature of the processor ( $T_{J,max}$ ). It is the responsibility of software to convert the relative temperature to an absolute temperature. The temperature returned by the DTS will always be at or below  $T_{J,max}$ . Catastrophic temperature conditions are detectable via an Out Of Spec status bit. This bit is also part of the DTS MSR. When this bit is set, the processor is operating out of specification and immediate shutdown of the system should occur. The processor operation and code execution is not guaranteed once the activation of the Out of Spec status bit is set.

The DTS-relative temperature readout corresponds to the Intel Thermal Monitor 1/Intel Thermal Monitor 2 trigger point. When the DTS indicates maximum processor core temperature has been reached, the Intel Thermal Monitor 1 or 2 hardware thermal control mechanism will activate. The DTS and Intel Thermal Monitor 1/Intel Thermal Monitor 2 temperature may not correspond to the thermal diode reading because the thermal diode is located in a separate portion of the die and thermal gradient between the individual core DTS. Additionally, the thermal gradient from DTS to thermal diode can vary substantially due to changes in processor power, mechanical and thermal attach, and software application. The system designer is required to use the DTS to guarantee proper operation of the processor within its temperature operating specifications.

Changes to the temperature can be detected via two programmable thresholds located in the processor MSRs. These thresholds have the capability of generating interrupts via the core's local APIC. Refer to the *Intel® 64 and IA-32 Architectures Software Developer's Manual* for specific register and programming details.



### 5.1.5 Out of Specification Detection

Overheat detection is performed by monitoring the processor temperature and temperature gradient. This feature is intended for graceful shut down before the THERMTRIP# is activated. If the processor's Intel Thermal Monitor 1 or 2 are triggered and the temperature remains high, an "Out Of Spec" status and sticky bit are latched in the status MSR register and generates thermal interrupt.

### 5.1.6 PROCHOT# Signal Pin

An external signal, PROCHOT# (processor hot), is asserted when the processor die temperature has reached its maximum operating temperature. If Intel Thermal Monitor 1 or 2 is enabled, then the TCC will be active when PROCHOT# is asserted. The processor can be configured to generate an interrupt upon the assertion or deassertion of PROCHOT#. Refer to the *Intel® 64 and IA-32 Architectures Software Developer's Manual* for specific register and programming details.

The processor implements a bi-directional PROCHOT# capability to allow system designs to protect various components from overheating situations. The PROCHOT# signal is bi-directional in that it can either signal when the processor has reached its maximum operating temperature or be driven from an external source to activate the TCC. The ability to activate the TCC via PROCHOT# can provide a means for thermal protection of system components.

Only a single PROCHOT# pin exists at a package level of the processor. When either core's thermal sensor trips, the PROCHOT# signal will be driven by the processor package. If only Intel Thermal Monitor 1 is enabled, PROCHOT# will be asserted and only the core that is above TCC temperature trip point will have its core clocks modulated. If Intel Thermal Monitor 2 is enabled, then regardless of which core(s) are above TCC temperature trip point, both cores will enter the lowest programmed Intel Thermal Monitor 2 performance state. It is important to note that Intel recommends both Intel Thermal Monitor 1 and 2 to be enabled.

When PROCHOT# is driven by an external agent, if only Intel Thermal Monitor 1 is enabled on both cores, then both processor cores will have their core clocks modulated. If Intel Thermal Monitor 2 is enabled on both cores, then both processor cores will enter the lowest programmed Intel Thermal Monitor 2 performance state. It should be noted that Force Intel Thermal Monitor 1 on Intel Thermal Monitor 2, enabled via BIOS, does not have any effect on external PROCHOT#. If PROCHOT# is driven by an external agent when Intel Thermal Monitor 1, Intel Thermal Monitor 2, and Force Intel Thermal Monitor 1 on Intel Thermal Monitor 2 are all enabled, then the processor will still apply only Intel Thermal Monitor 2.

PROCHOT# may be used for thermal protection of voltage regulators (VR). System designers can create a circuit to monitor the VR temperature and activate the TCC when the temperature limit of the VR is reached. By asserting PROCHOT# (pulled-low) and activating the TCC, the VR will cool down as a result of reduced processor power consumption. Bi-directional PROCHOT# can allow VR thermal designs to target maximum sustained current instead of maximum current. Systems should still provide proper cooling for the VR and rely on bi-directional PROCHOT# only as a backup in case of system cooling failure. The system thermal design should allow the power delivery circuitry to operate within its temperature specification even while the processor is operating at its TDP. With a properly designed and characterized thermal solution, it is anticipated that bi-directional PROCHOT# would only be asserted for very short periods of time when running the most power intensive applications. An under-designed thermal solution that is not able to prevent excessive assertion of PROCHOT# in the anticipated ambient environment may cause a noticeable performance loss.

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